swissbit®

Product data sheet

Industrial CompactFlash Card

C-100 Series

up to MDMA4 / PIO6

Standard and industrial temperature grade

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128Mbyte, 256MByte, 512MByte, 1GByte, 2GByte, 4GByte and 8GByte 3.3/5V Supply CompactFlash™ Card

1 Features

- Custom-designed, highly-integrated memory controller
  - Fully compliant with CompactFlash™ specification 3.0
  - Fully compatible with PCMCIA specification
  - PC Card ATA Interface supported
  - True IDE mode compatible
  - Up to PIO mode 6 supported
  - Up to Multi-Word DMA4
  - Hardware RS-code ECC (4 Bytes/528 Bytes correction)
  - Removable or fix drive
- Small form factor
  - 36.4mm x 42.8mm x 3.3mm
- Low-power CMOS technology
- 3.3V / 5.0V power supply
- Power saving mode (with Automatic Wake-up)
- Endurance
  - 10 years data retention
  - Wear leveling
  - Endurance: ~2,000,000 erase / write cycles depends on use case
  - Read unlimited
- High reliability
  - MTBF > 3,000,000 hours
  - Data reliability: < 1 non-recoverable error per 10^{14} bits read
  - Number of card insertions/removals: >10,000
- Hot swappable
- Controlled BOM

- High performance
  - Up to 16.7MB/s burst transfer rate in PIO4 or 25MB/s in PIO6
  - Sustained Write performance (host to Card): up to 12.7MB/s
  - Sustained Read Performance (Host to Card: up to 18MB/s in USB card reader)
- Available densities
  - up to 8 GBytes
- Operating System support
  - Standard Software Drivers operation Compact Flash

2 Table of Contents

3 Order Information

IDE-FIX & PCMCIA-REMOVABLE / PIO & DMA support / 0°C – +70°C

Density	Part Number
128MB	SFCF0128HxBI1SA-C-M0-532-STD
256MB	SFCF0256HxBI1SA-C-M0-532-STD
512MB	SFCF0512HxBI2SA-C-M0-532-STD
1GB	SFCF1024HxBI2SA-C-M0-532-STD
2GB	SFCF2048HxBI2SA-C-D0-532-STD
4GB	SFCF4096HxBI2SA-C-Q1-532-STD
8GB	SFCF8192HxBI4SA-C-Q1-532-STD

Table 1: Standard product list – commercial temperature

IDE-FIX & PCMCIA-REMOVABLE / PIO & DMA support / -40°C – +85°C

Density	Part Number
128MB	SFCF0128HxBI1SA-I-M0-532-STD
256MB	SFCF0256HxBI1SA-I-M0-532-STD
512MB	SFCF0512HxBI2SA-I-M0-532-STD
1GB	SFCF1024HxBI2SA-I-M0-532-STD
2GB	SFCF2048HxBI2SA-I-D0-532-STD
4GB	SFCF4096HxBI2SA-I-Q1-532-STD
8GB	SFCF8192HxBI4SA-I-Q1-532-STD

Table 2: Standard product list – industrial temperature
x= depends on product generation

3.1 Offered options

- Removable or fixed drive
- Disabling DMA mode option
- Up to PIO6 (25MB/s burst) and up to DMA4
- Customer specified card size and card geometry (C/H/S – cylinder/head/sector)
- Customer specified strings and IDs
- Preload service
- Customized labels
- 2 Temperature ranges
  - Commercial Temperature range 0 ... +70°C
  - Industrial Temperature range -40 ... +85°C
- ROM mode (write protected with uploaded software)
- Option for special FW like:
  - write protection with password
  - read out current bad blocks for life time estimation
  - delaying the switch between PC Card ATA and True-IDE mode
  - Phoenix-BIOS (Word 49 Bit 11 of Drive ID)

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4 Product Specification

The CompactFlash is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The Card operates in three basic modes [1]:

- **PC Card ATA I/O mode**
- **PC Card ATA memory mode**
- **True IDE mode**

The CompactFlash also supports Advanced Timing modes. Advanced Timing modes are ATA I/O modes that are 100ns or faster, ATA Memory modes that are 100ns or 80ns.
Standard cards are shipped as max. **PIO6 and MDMA4 (80ns).**
In standard True IDE interface only PIO4 and MDMA2 (120ns) is specified.
If the cards should be used in extended speed modes, they should be qualified on the target system and the system should **fulfill the requirements** listed below.
It conforms to the PC Card Specification when operating in the ATA I/O mode, and in the ATA Memory mode (Personal Computer Memory Card International Association standard, JEIDA in Japan), and to the ATA specification when operating in True IDE Mode. CompactFlash Cards can be used with passive adapters in a PC-Card Type II or Type III socket.
The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC)**, **defect handling, diagnostics and clock control**.
The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.
Once the Card has been configured by the host, it behaves as a standard ATA (IDE) disk drive. The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.
The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down.
The specification has been realized and approved by the CompactFlash Association (CFA).
This non-proprietary specification enables users to develop CF products that function correctly and are compatible with future CF design.

Related Documentation

- PCMCIA PC Card Standard, 1995
- PCMCIA PC Card ATA Specification, 1995
- AT Attachment Interface Document, American National Standards Institute, X3.221-1994
- CF+ and CompactFlash Specification Revision 3.0

The CF card switches between the modes depending on the state of Pin 9 of the card at power on.
The decision can be optional delayed by some hundreds of ms, if the host system does not fulfill the specification and sets the correct state of pin 9 later.

The main differences between the modes are:

	PC Card ATA	True IDE
Pin9 (-OE) at power on	high	low
Pin41 (Reset)	high active	low active
CIS (Card information structure)	yes	no

Details in the electrical interface specification (Chapter 5) and Command interface specification (Chapter 6)

4.1 System Performance

Table 3: System Performance

System Performance		Typical	Unit
Power-On to Ready		540(1)	ms
Reset to Ready		500(1)	ms
Sleep to Ready		1.9(1)	µs
Sleep to write (Power Down to Ready + Write Command to DRQ)		35(1)	µs
Sleep to read (Power Down to Ready + Read Command to DRQ)		110(1)	µs
Command to DRQ (Sector Read at Ready state)		107.5(1)	µs
Command to DRQ (Sector Write at Ready state)		33.2(1)	µs
Data transfer cycle end to ready (Sector Write)		336(1)	µs
Auto Power-down time		110(1)	ms
Transfer Rates		**max.**	**Unit**
Data transfer Rate (burst)	PIO4 / MDMA2	16.6 (110X)(2)(3)	MB/s
	PIO6 / MDMA4	25 (166X)(2)(3)	
Sustained Read	256MB	12 (80X) (2)(4)	
	512MB – 8GB	18 (120X) (2)(4)	
Sustained Write	256MB	6 (40X) (2)(4)	
	512MB – 8GB	13 (87X) (2)(4)	

(1) 1x Flash 2k SLC / 40MHz / PIO6
(2) ...X are speed grade markings where 1X = 150 kByte/s. All values refer to Samsung SLC Flash CompactFlash Card in MDMA4 mode, cycle time 80ns, sequential write / read in CF-USB card reader.
(3) True IDE is specified up to PIO4 / MDMA2
(4) Sustained Speed depends on flash type and number, file size, and burst speed

Requirements for using extended speed (PIO 5, 6/ DMA 3, 4)

(CompactFlash Specification 3.0)

The CF Advanced Timing modes include PCMCIA I/O and Memory modes that are 100ns or faster and True IDE PIO Modes 5, 6 and Multiword DMA Modes 3, 4.

When operating in CF Advanced timing modes, the host shall conform to the following requirements:

1. Only one CF device shall be attached to the CF Bus.
2. The host shall not present a load of more than 40pF to the device for all signals, including any cabling.
3. The maximum cable length is 0.05 m (2 in). The cable length is measured from the card connector to the host controller. 0.46 m (18 in) cables are not supported.
4. The –WAIT and IORDY signals shall be ignored by the host.

Devices supporting CF Advanced timing modes shall also support slower timing modes, to ensure operability with systems that do not support CF Advanced timing modes.

4.2 Environmental Specifications

4.2.1 Recommended Operating Conditions

Table 4: CF Card Recommended Operating Conditions

Parameter	Value
Commercial Operating Temperature	0°C to 70°C
Industrial Operating Temperature	-40°C to 85°C
Power Supply VCC Voltage (5V)	4.5V to 5.5V – 5.0V ±10%
Power Supply VCC Voltage (3.3V)	2.97V to 3.63V – 3.3V ±10%

Table 5: Current consumption (1)

Current Consumption (type)	3.3V	5V	Unit
Read (typ / max)	40 / 50	45 / 70	mA
Write (typ / max)	40 / 50	45 / 90	
Sleep/Idle Mode (typ / max)	0.7 / 1.5	4 / 6	

1. All values are typical at 25° C and nominal supply voltage and refer to 1Gbyte CompactFlash Card in MDMA2 mode.
   Max values are for 8GB cards in MDMA4 mode in IDE mode.
   The card goes to Sleep/idle mode 100ms after last host command.

4.2.2 Recommended Storage Conditions

Table 6: CF Card Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-65°C to 150°C
Industrial Storage Temperature	-65°C to 150°C

4.2.3 Shock, Vibration, and Humidity

Table 7: Shock, Vibration, and Humidity

Parameter	Value
Humidity (non-condensing)	85% RH 85°C, 1000 hrs (JEDEC JESD22, method A101-B)
Vibration	20 G peak, 20-2000Hz, 4 per direction (JEDEC JESD22, method B103) 5.35G RMS, 15 min per plane (IEC 68-2-6)
Shock	1.5k G peak, 0.5ms 5 times (JEDEC JESD22, method B110) 30 G, 11ms 1 time (IEC 68-2-27)

4.3 Physical Dimensions

Table 8: Physical Dimensions

Physical Dimensions		Unit
Width	42.8	mm
Height	36.4	
Thickness	3.3	
Weight (typ.)	10	g

4.4 Reliability

Table 9: System Reliability and Maintenance

Parameter	Value
MTBF (at 25°C)	> 3,000,000 hours
Insertions/Removals	> 10,000
Data Reliability	< 1 Non-Recoverable Error per 10^{14} bits Read
Data Retention	10 years

1 Dependent on final system qualification data.

4.5 Drive Geometry / CHS Parameter

Table 10: CF capacity specification

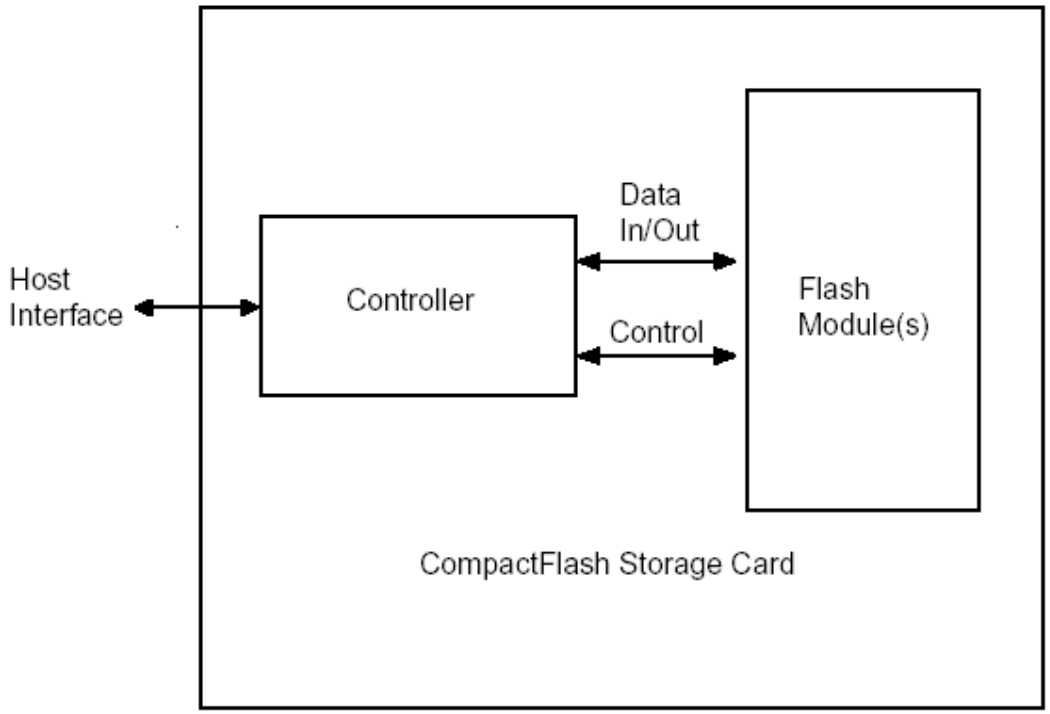
Capacity	Default_cylinders	Default_heads	Default_sectors _track	Sectors_card	Total addressable capacity (Byte)
32MB	496	4	32	63,488	32,505,856
64MB	490	8	32	125,440	64,225,280
128MB	980	8	32	250,880	128,450,560
256MB	980	16	32	501,760	256,901,120
512MB	993	16	63	1,000,944	512,483,328
1GB	1,986	16	63	2,001,888	1,024,966,656
2GB	3,970	16	63	4,001,760	2,048,901,120
4GB	7,964	16	63	8,027,712	4,110,188,544
8GB	15,880	16	63	16,007,040	8,195,604,480
16GB	16,383 (1)	15	63	31,717,728	16,239,476,736

(1) The CHS addressing is limited to about 8GB. Larger drives should be used in LBA mode

4.6 Physical description

The CompactFlash Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s). Figure 1 shows the Block Diagram of the CompactFlash Memory Card.
The Card is offered in a Type I package with a 50-pin connector consisting of two rows of 25 female contacts on 50 mil (1.27mm) centers. Figure 10 shows Type I Card Dimensions.

Figure 1: CompactFlash Memory Card Block Diagram



5 Electrical interface

5.1 Electrical description

The CompactFlash Memory Card operates in three basic modes:

- PC Card ATA using I/O Mode
- PC Card ATA using Memory Mode
- True IDE Mode, which is compatible with most disk drives

The signal/pin assignments are listed in Table 11 Low active signals have a '-' prefix. Pin types are Input, Output or Input/Output.
The configuration of the Card is controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the memory card.
Table 12 describes the I/O signals. Inputs are signals sourced from the host while Outputs are signals sourced from the Card. The signals are described for each of the three operating modes.
All outputs from the Card are totem pole except the data bus signals that are bi-directional tri-state. Refer to the section titled "Electrical Specifications" for definitions of Input and Output type.

Table 11: Pin Assignment and Pin Type

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
1	GND		Ground	GND		Ground	GND		Ground
2	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	-CE1	I	I3U	-CS0	I	I3Z
8	A10	I	I1Z	A10	I	I1Z	A10(2)	I	I1Z
9(1)	-OE	I	I3U	-OE	I	I3U	-ATASEL	I	I3U
10	A09	I	I1Z	A09	I	I1Z	A09(2)	I	I1Z
11	A08	I	I1Z	A08	I	I1Z	A08(2)	I	I1Z
12	A07	I	I1Z	A07	I	I1Z	A07(2)	I	I1Z
13	Vcc		Power	Vcc		Power	Vcc		Power
14	A06	I	I1Z	A06	I	I1Z	A06(2)	I	I1Z
15	A05	I	I1Z	A05	I	I1Z	A05(2)	I	I1Z
16	A04	I	I1Z	A04	I	I1Z	A04(2)	I	I1Z
17	A03	I	I1Z	A03	I	I1Z	A03(2)	I	I1Z
18	A02	I	I1Z	A02	I	I1Z	A02	I	I1Z
19	A01	I	I1Z	A01	I	I1Z	A01	I	I1Z
20	A00	I	I1Z	A00	I	I1Z	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3	D02	I/O	I1Z,OZ3
24	WP	0	OT3	-IOIS16	0	OT3	-IOIS16	0	ON3
25	-CD2	0	Ground	-CD2	0	Ground	-CD2	0	Ground
26	-CD1	0	Ground	-CD1	0	Ground	-CD1	0	Ground
27	D11(3)	I/O	I1Z,OZ3	D11(3)	I/O	I1Z,OZ3	D11(3)	I/O	I1Z,OZ3
28	D12(3)	I/O	I1Z,OZ3	D12(3)	I/O	I1Z,OZ3	D12(3)	I/O	I1Z,OZ3
29	D13(3)	I/O	I1Z,OZ3	D13(3)	I/O	I1Z,OZ3	D13(3)	I/O	I1Z,OZ3
30	D14(3)	I/O	I1Z,OZ3	D14(3)	I/O	I1Z,OZ3	D14(3)	I/O	I1Z,OZ3

Pin Num	PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type	Signal Name	Pin Type	In, Out Type
31	D15(3)	I/O	I1Z,0Z3	D15(3)	I/O	I1Z,0Z3	D15(3)	I/O	I1Z,0Z3
32	-CE2(3)	I	I3U	-CE2(3)	I	I3U	-CS1(3)	I	I3Z
33	-VS1	O	Ground	-VS1	O	Ground	-VS1	O	Ground
34	-IORD	I	I3U	-IORD	I	I3U	-IORD	I	I3Z
35	-IOWR	I	I3U	-IOWR	I	I3U	-IOWR	I	I3Z
36	-WE	I	I3U	-WE	I	I3U	-WE(4)	I	I3U
37	READY	O	OT1	-IREQ	O	OT1	INTRQ	O	OZ1
38	Vcc		Power	Vcc		Power	Vcc		Power
39	-CSEL(5)(3)	I	I2Z	-CSEL(5)	I	I2Z	-CSEL(5)	I	I2U
40	-VS2	O	OPEN	-VS2	O	OPEN	-VS2	O	OPEN
41	RESET	I	I2Z	RESET	I	I2Z	-RESET	I	I2Z
42	-WAIT	O	OT1	-WAIT	O	OT1	IORDY	O	ON1
43	-INPACK	O	OT1	-INPACK	O	OT1	DMARQ	O	OZ1
44	-REG	I	I3U	-REG	I	I3U	-DMACK(6)	I	I3U
45	BVD2	I/O	I1U,OT1	-SPKR	I/O	I1U,OT1	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1U,OT1	-STSCHG	I/O	I1U,OT1	-PDIAG	I/O	I1U,ON1
47	D08(3)	I/O	I1Z,0Z3	D08(3)	I/O	I1Z,0Z3	D08(3)	I/O	I1Z,0Z3
48	D09(3)	I/O	I1Z,0Z3	D09(3)	I/O	I1Z,0Z3	D09(3)	I/O	I1Z,0Z3
49	D10(3)	I/O	I1Z,0Z3	D10(3)	I/O	I1Z,0Z3	D10(3)	I/O	I1Z,0Z3
50	GND		Ground	GND		Ground	GND		Ground

1. For True IDE Mode, pin 9 is grounded.
2. The signal should be grounded by the host.
3. These signals are required only for 16 bit accesses and not required when installed in 8 bit systems. Devices should allow for 3-state signals not to consume current.
4. The signal should be tied to Vcc by the host.
5. The –CSEL signal is ignored by the Card in PC Card modes. However, because it is not pulled up on the Card in these modes it should not be left floating by the host in PC Card modes. In these modes, the pin is normally connected by the host to PC Card A25 or grounded by the host.
6. When the device does not operate in DMA mode, the signal should be held high or tied to Vcc by the host. To ensure proper operation with older hosts when DMA mode is disabled, the Card should ignore the –DMACK signal.

Table 12: Signal Description

Signal Name	Dir.	Pin	Description
A10 to A0 (PC Card Memory Mode)	I	8,10,11,12, 14,15,16,17, 18,19,20	Used (with –REG) to select: the I/O port address registers, the memory mapped port address registers, a Byte in the Card information structure and its configuration control and status registers.
A10 to A0 (PC Card I/O Mode)			Same as PC Card Memory Mode
A2 to A0 (True IDE Mode)			Only A2 to A0 are used to select the one of eight registers in the Task File, the remaining lines should be grounded.
BVD1 (PC Card Memory Mode)	I/O	46	The battery voltage status of the Card, as no battery is required it is asserted High.
–STSCHG (PC Card I/O Mode)			Alerts the host to changes in the READY and Write Protect states. Its use is controlled by the Card Configuration and Status Register.
–PDIAG (True IDE Mode)			The Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (PC Card Memory Mode)	I/O	45	The battery voltage status of the Card, as no battery is required it is asserted High.
–SPKR (PC Card I/O Mode)			The Binary Audio output from the Card. It is asserted High as audio functions are not supported.

Signal Name	Dir.	Pin	Description
–DASP (True IDE Mode)			This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
D15–D00 (PC Card Memory Mode)	I/O	31, 30, 29, 28, 27, 49, 48, 47, 6, 5, 4, 3, 2, 23, 22, 21	Carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15–D00 (PC Card I/O Mode)			Same as PC Card Memory Mode.
D15–D00 (True IDE Mode)			All Task File operations occur in Byte mode on D00 to D07 while all data transfers are 16 bit using D00 to D15.
GND (PC Card Memory Mode)		1, 50	Ground.
GND (PC Card I/O Mode)			Same for all modes.
GND (True IDE Mode)			Same for all modes.
–INPACK (PC Card Memory Mode)	0	43	Not used, should not be connected to the host.
–INPACK (PC Card I/O Mode)			The Input Acknowledge is asserted when the Card is selected and responding to an I/O read cycle at the current address on the bus. It is used by the host to control the enable of any input data buffers between the Card and CPU.
DMARQ (True IDE Mode)			The DMARQ input signal is used to request a DMA data transfer between the host and the Card. It is asserted to notify that the Card is ready to transfer data to or from the host. For Multi-Word DMA transfers, the direction of data transfer is controlled by –IORD and –IOWR. DMARQ is used in conjunction with –DMACK to perform handshaking: the Card waits until –DMACK has been asserted by the host to de-assert DMARQ, and re-assert it again if there is still data to be transferred (see Section 10.10). DMARQ is not driven when the Card is not selected. If the host does not support DMA mode, DMARQ should be left unconnected.
–IORD (PC Card Memory Mode)	I	34	Not used.
–IORD (PC Card I/O Mode)			I/O Read strobe generated by the host. It gates I/O data onto the bus.
–IORD (True IDE Mode)			Same as PC Card I/O Mode.
–CD1, –CD2 (PC Card Memory Mode)	0	26, 25	These are connected to ground on the Card. They are used by the host to determine that the Card is fully inserted into its socket.
–CD1, –CD2 (PC Card I/O Mode)			Same for all modes.
–CD1, –CD2 (True IDE Mode)			Same for all modes.
–CE1, –CE2 (PC Card Memory Mode)	I	7, 32	Used to select the Card and to indicate whether a Byte or a Word operation is being performed. –CE2 accesses the odd Byte; –CE1 accesses the even Byte or the odd Byte depending on A0 and –CE2. A multiplexing scheme based on A0, –CE1, –CE2 allows 8 bit hosts to access all data on D0 to D7.
–CE1, –CE2 (PC Card I/O Mode)			Same as PC Card Memory Mode.
–CS0, –CS1 (True IDE Mode)			–CS0 is the chip select for the task file registers, while –CS1 selects the Alternate Status Register and the Device Control Register. When –DMACK is asserted, –CS0 and –CS1 must be reasserted and data width is 16 bits.
–CSEL (PC Card Memory Mode)	I	39	Not used.
–CSEL (PC Card I/O Mode)			Not used.

Signal Name	Dir.	Pin	Description
–CSEL (True IDE Mode)			This internally pulled up signal is used to configure the Card as a Master or Slave. When grounded it is configured as a Master, when open it is configured as a Slave.
–IOWR (PC Card Memory Mode)	I	35	Not used.
–IOWR (PC Card I/O Mode)			The I/O Write strobe pulse is used to clock I/O data on the bus into the Card controller registers. Clocking occurs on the rising edge.
–IOWR (True IDE Mode)			Same as PC Card I/O Mode.
–OE (PC Card Memory Mode)	I	9	This is an Output Enable strobe generated by the host interface. It reads data and the CIS and configuration registers.
–OE (PC Card I/O Mode)			Reads the CIS and configuration registers.
–ATASEL (True IDE Mode)			This input signal must be driven Low to enable True IDE mode.
READY (PC Card Memory Mode)	O	37	Indicates whether the Card is busy (Low), or ready to accept a new data transfer operation (High). The Host socket must provide a pull-up resistor. At power up and Reset, the READY signal is held Low until the commands are completed. No access should be made during this time. The READY signal is held High whenever the Card has been powered up with RESET continuously disconnected or asserted.
–IREQ (PC Card I/O Mode)			Interrupt Request. It is strobed Low to generate a pulse mode interrupt or held Low for a level mode interrupt.
INTRQ (True IDE Mode)			Active High Interrupt Request to the host.
–REG (PC Card Memory Mode)	I	44	Used to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.
–REG (PC Card I/O Mode)			Must be Low during I/O Cycles when the I/O address is on the Bus.
–DMACK (True IDE Mode)			The –DMACK input signal is used to acknowledge DMA transfers. It is asserted by the host in response to DMARQ to initiate the transfer. When DMA mode is disabled, the Card should ignore the –DMACK signal. If the host does not support DMA mode, but only True IDE mode, this signal should be driven High or tied to Vcc by the host.
RESET (PC Card Memory Mode)	I	41	Resets the Card (active High). The Card is Reset at power up only if this pin is left High or unconnected.
RESET (PC Card I/O Mode)			Same as PC Card Memory Mode.
–RESET (True IDE Mode)			Hardware Reset from the host (active Low).
Vcc (PC Card Memory Mode)		13, 38	+5V, +3.3V power.
Vcc (PC Card I/O Mode)			Same for all modes.
Vcc (True IDE Mode)			Same for all modes.
–VS1, –VS2 (PC Card Memory Mode)	O	33, 40	Voltage Sense Signals. –VS1 is grounded so that the CIS can be read at 3.3 volts and –VS2 is reserved by PCMCIA for a secondary voltage.
–VS1, –VS2 (PC Card I/O Mode)			Same for all modes.
–VS1, –VS2 (True IDE Mode)			Same for all modes.
–WAIT (PC Card Memory Mode)	O	42	ST CF does not assert the WAIT (IORDY) signal
–WAIT (PC Card I/O Mode)			

Signal Name	Dir.	Pin	Description
IORDY (True IDE Mode)			
–WE (PC Card Memory Mode)	I	36	Driven by the host to strobe memory write data to the registers.
–WE (PC Card I/O Mode)			Used for writing to the configuration registers.
–WE (True IDE Mode)			Not used, should be connected to Vcc by the host.
WP (PC Card Memory Mode)	O	24	No write protect switch available. It is held Low after the completion of the reset initialization sequence.
–IOIS16 (PC Card I/O Mode)			Used for the 16 bit Port (–IOIS16) function. Low indicates that a 16 bit or odd Byte only operation can be performed at the addressed port.
–IOCS16 (True IDE Mode)			Asserted Low when the Card is expecting a Word data transfer cycle.

5.2 Electrical Specification

Table 13 defines the DC Characteristics for the CompactFlash Memory Card. Unless otherwise stated, conditions are:

- Vcc = 5V ± 10%
- Vcc = 3.3V ± 5%
- -40 °C to +85 °C

Table 14 shows that the Card operates correctly in both the voltage ranges and that the current requirements must not exceed the maximum limit shown.

Table 13: Absolute Maximum Conditions

Parameter	Symbol	Conditions
Input Power	VCC	-0.3V to 6.5V
Voltage on any pin except VCC with respect to GND	V	~ -0.5V to VCC +0.5V

Table 14: Input Power

Voltage	Maximum Average RMS Current	Measurement Conditions
3.3V ±5%	45mA	-40... +85 °C
5V ±10%	50mA	-40... +85°C

5.3 Current Measurement

The current is measured by connecting an amp meter in series with the Vcc supply. The meter should be set to the 2A scale range, and have a fast current probe with an RC filter with a time constant of 0.1ms. Current measurements are taken while looping on a data transfer command with a sector count of 128. Current consumption values for both read and write commands are not to exceed the Maximum Average RMS Current specified in Table 14. Table 15 shows the Input Leakage Current, Table 16 the Input Characteristics, Table 17 the Output Drive Type and Table 18 the Output Drive Characteristics.

Table 15: Input Leakage current[1]

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
IxZ	Input Leakage Current	IL	V_{IH} =Vcc V_{IL} = GND	-1		1	µA
IxU	Pull Up Resistor	RPU1	Vcc = 5.0V	50		500	kOhm
IxD	Pull Down Resistor	RPD1	Vcc = 5.0V	50		500	kOhm

1. x refers to the characteristics described in Table 16 For example, I1U indicates a pull up resistor with a type 1 input characteristic.

Table 16: Input characteristics

Type	Parameter	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
			Vcc = 3.3V			Vcc = 5.0V			
1	Input Voltage CMOS	V_{IH}	2.4			3.3			V
		V_{IL}			0.6			0.8	
2	Input Voltage CMOS	V_{IH}	1.5			2.0			V
		V_{IL}			0.6			0.8	
3	Input Voltage CMOS Schmitt Trigger	V_{TH}		1.8			2.8		V
		V_{TL}		1.0			2.0		

Table 17: Output Drive Type[1]

Type	Output Type	Valid Conditions
0tx	Totempole	I_{OH} & I_{OL}
0zx	Tri-State N-P Channel	I_{OH} & I_{OL}
0px	P-Channel Only	I_{OH} only
0nx	N-Channel Only	I_{OL} only

1. x refers to the characteristics described in Table 18 For example, 0T3 refers to totem pole output with a type 3 output drive characteristic.

Table 18: Output Drive Characteristics

Type	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
1	Output Voltage	V_{OH}	I_{OH}= -4mA	Vcc -0.8V			V
		V_{OL}	I_{OL} = 4mA			Gnd + 0.4V	
2	Output Voltage	V_{OH}	I_{OH} = -4mA	Vcc -0.8V			V
		V_{OL}	I_{OL} = 4mA			Gnd + 0.4V	
3	Output Voltage	V_{OH}	I_{OH}= -4mA	Vcc -0.8V			V
		V_{OL}	I_{OL} = 4mA			Gnd + 0.4V	
	Tri-State	I_{OZ}	V_{OL}= Gnd	-10		10	µA
X	Leakage Current		V_{OH} = Vcc				

5.4 Additional requirements for CompactFlash Advanced Timing mode

When operating in a CompactFlash Advanced timing mode, the following conditions must be respected:

- **Only one CompactFlash Card must be connected to the CompactFlash bus.**
- The load capacitance (cable included) for all signals must be lower than 40pF.
- The cable length must be **lower than 0.15m** (6 inches). The cable length is measured from the Card connector to the host controller. **0.46m (18 inches) cables are not supported**.

6 Command Interface

There are two types of bus cycles and timing sequences that occur in the PCMCIA type interface, direct mapped I/O transfer and memory access. Two types of bus cycles are also available in True IDE interface type: PIO transfer and Multi-Word DMA transfer.

Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, and Table 26 show the read and write timing parameters. Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 and Figure 9 show the read and write timing diagrams.

In order to set the card mode, the –OE (-ATASEL) signal must be set and kept stable before applying VCC until the reset phase is completed. To place the card in Memory mode or I/O mode, -OE (-ATASEL) must be driven High, while it must be driven Low to place the card in True IDE mode.

6.1 Attribute Memory Read and Write

Figure 2: Attribute Memory Read waveforms

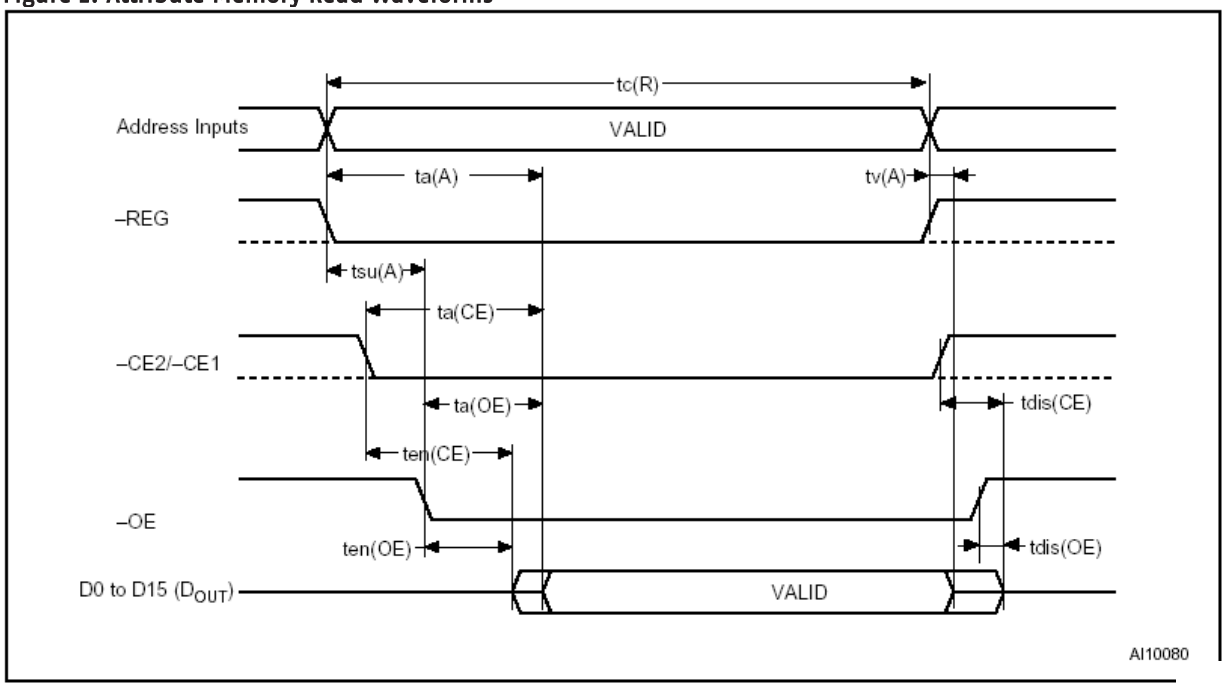
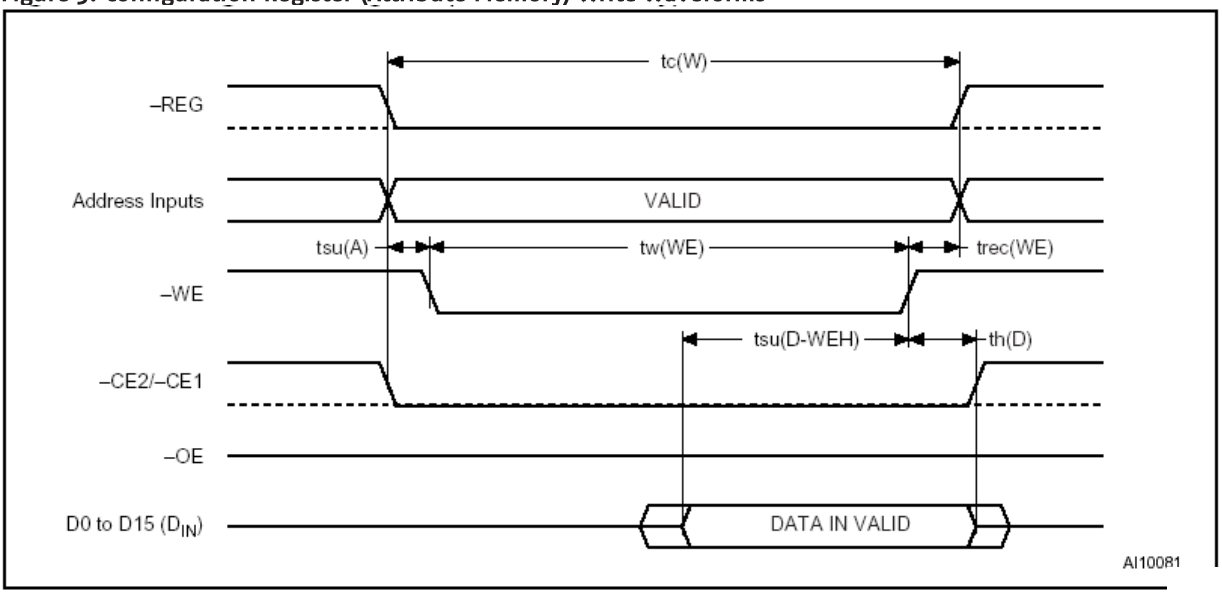


Table 19: Attribute Memory Read timing

Speed version			300ns	
Item	**Symbol**	**IEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Read Cycle Time	tcl	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	
Address Setup Time	tsu(A)	tAVWL	30	

Figure 3: Configuration Register (Attribute Memory) Write waveforms



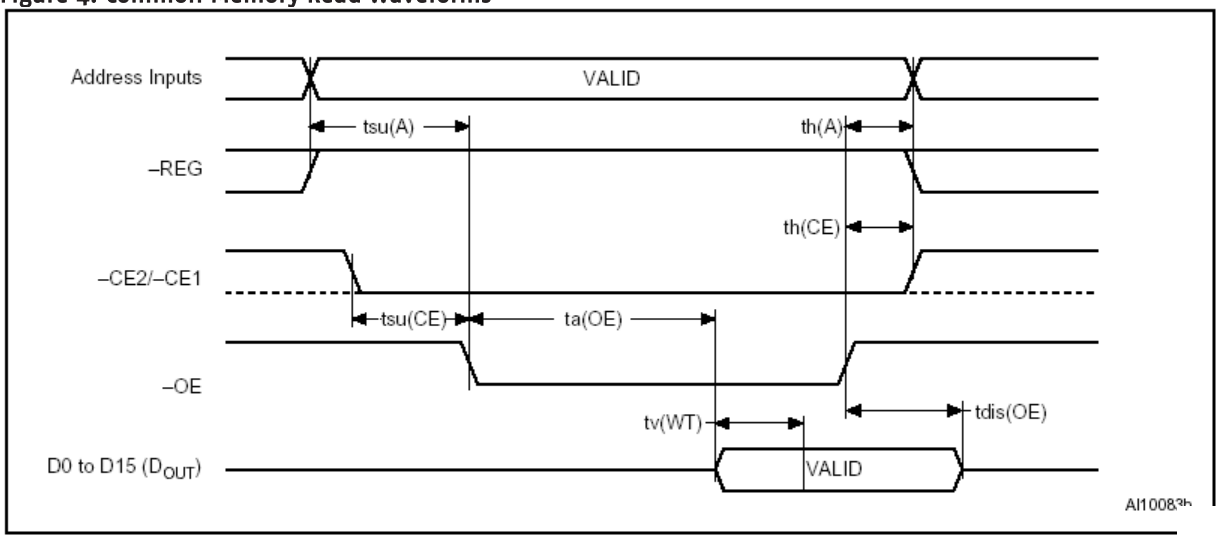
- D_{IN} signifies data provided by the system to the CompactFlash Card.

Table 20: Configuration Register (Attribute Memory) Write timing

Speed Version			250ns	
Item	**Symbol**	**IEEEE Symbol**	**Min. (ns)**	**Max. (ns)**
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	
Write Recovery Time	trec(WE)	tWMAX	30	

6.2 Common Memory Read and Write

Figure 4: Common Memory Read waveforms



- D_{OUT} means data provided by the CompactFlash Memory Card to the system.

Table 21: Common Memory Read timing [1]$

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)	tGLQV		125		60		50		45
Output Disable Time from OE	tdis(OE)	tGHQZ		100		60		50		45
Address Setup Time	tsu(A)	tAVGL	30		15		10		10	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Setup before OE	tsu(CE)	tELGL	0		0		0		0	
CE Hold following OE	th(CE)	tGHEH	20		15		15		10	

- Swissbit CF does not assert the WAIT signal.

Figure 5: Common Memory Write Waveforms

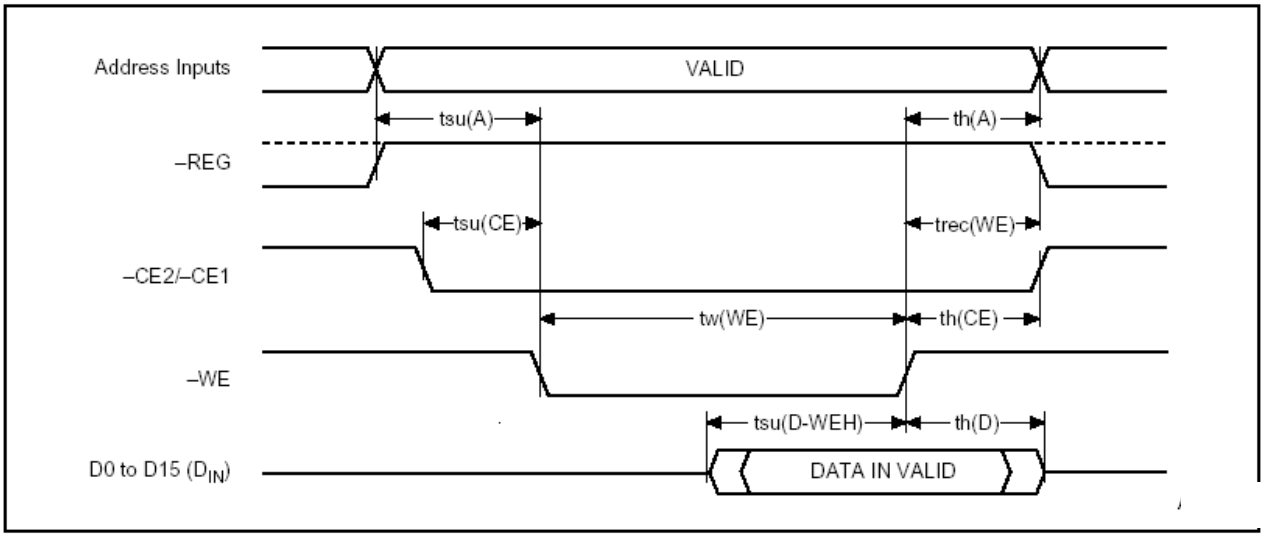


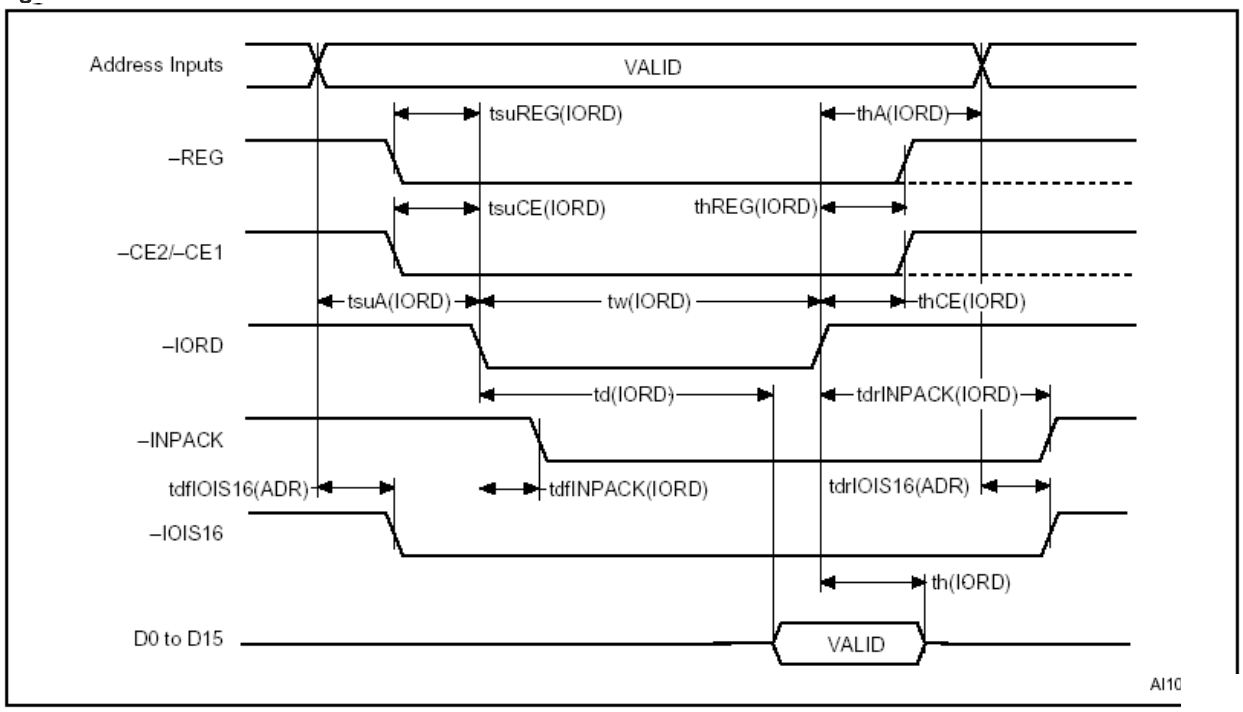
Table 22: Common Memory Write Timing[1]

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80		50		40		30	
Data Hold following WE	th(D)	tIWMDX	30		15		10		10	
WE Pulse Width	tw(WE)	tWLWH	150		70		60		55	
Address Setup Time	tsu(A)	tAVWL	30		15		10		10	
CE Setup before WE	tsu(CE)	tELWL	0		0		0		0	
Write Recovery Time	trec(WE)	tWMAX	30		15		15		15	
Address Hold Time	th(A)	tGHAX	20		15		15		10	
CE Hold following WE	th(CE)	tGHEH	20		15		15		10	

- Swissbit CF does not assert the WAIT signal.

6.3 I/O Read and Write

Figure 6: I/O Read waveforms



- DOUT signifies data provided by the CompactFlash Memory Card or to the system.

Table 23: I/O Read timing[1]

Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100		50		50		45
Data Hold following IORD	th(IORD)	tIGHQX	0		5		5		5	
IORD Width Time	tw(IORD)	tIGLIGH	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		25		25		15	
Address Hold following IORD	thA(IORD)	tIGHAX	20		10		10		10	
CE setup before IORD	tsuCE(IORD)	tELIGL	5		5		5		5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20		10		10		10	
REG setup before IORD	tsuREG(IORD)	tRGLIGL	5		5		5		5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		0		0		0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	0	NA[2]	0	NA[2]	0	NA[2]
NPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45		NA[2]		NA[2]		NA[2]
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35						
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35						

1. Swissbit CF does not assert the WAIT signal.
2. –IOIS16 is not supported in this mode.

Figure 7: I/O Write waveforms

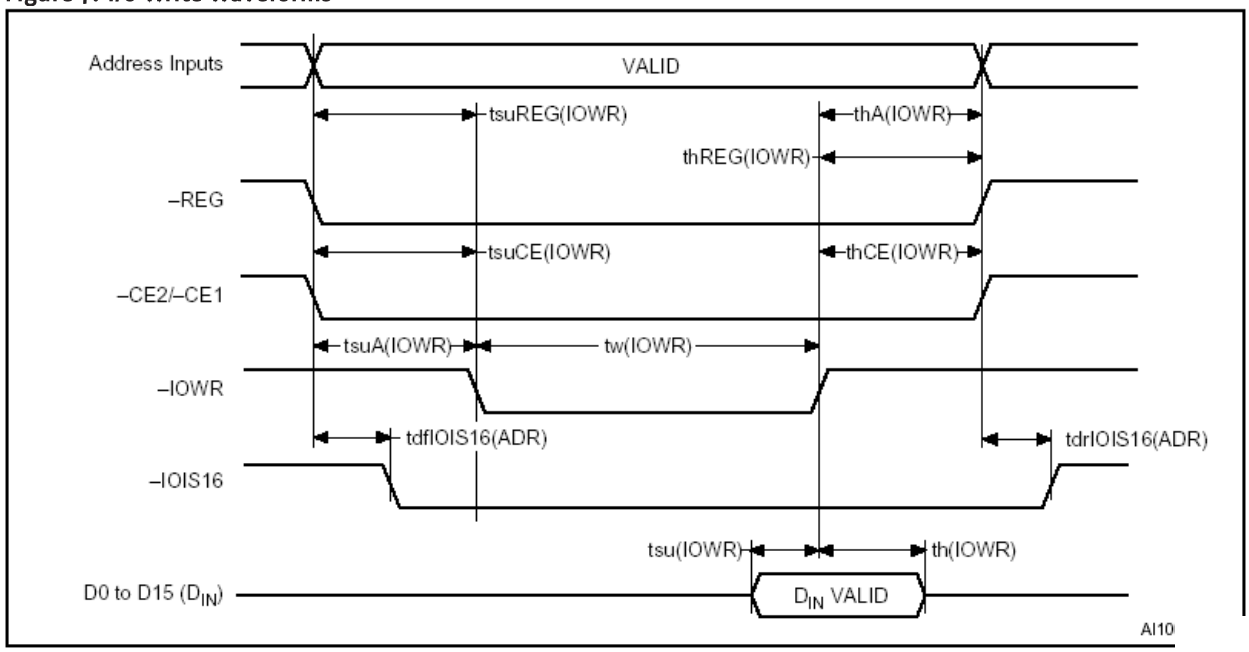


Table 24: I/O write timing

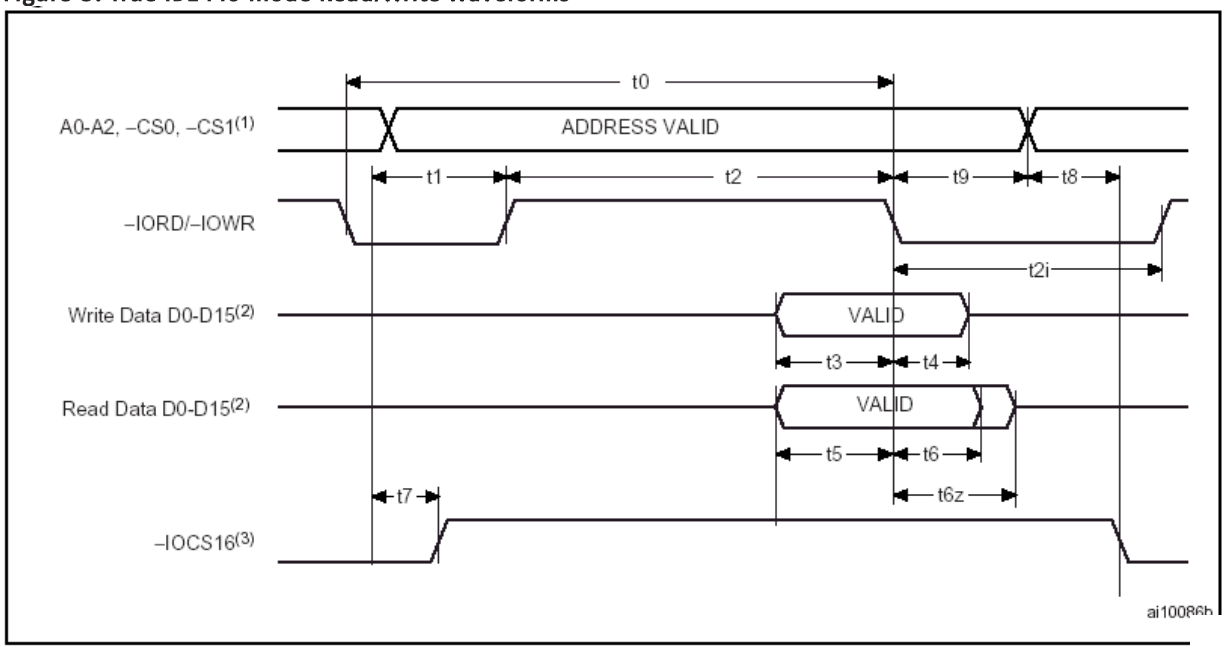
Cycle Time Mode			250ns		120ns		100ns		80ns	
Item	Symbol	IEEEE Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		20		20		15	
Data Hold following IOWR	th(IOWR)	tIWHDX	30		10		5		5	
IOWR Width Time	tw(IOWR)	tIWLIWH	165		70		65		55	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		25		25		15	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		20		10		10	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5		5		5		5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		20		10		10	
REG setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		5		5		5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		0		0		0	
IOIS16 Delay Falling from Addr.	tdfIOIS16(ADR)	tAVISL		35		NA(2)		NA(2)		NA(2)
IOIS16 Delay Rising from Addr.	tdrIOIS16(ADR)	tAVISH		35		NA(2)		NA(2)		NA(2)

1. D_{IN} signifies data provided by the system to the CompactFlash Memory Card or CF+ Card.
2. –IOIS16 and –INPACK are not supported in this mode.

6.4 True IDE Mode

The timing waveforms for True IDE mode and True IDE DMA mode of operation in this section are drawn using the conventions in the ATA-4 specification, which are different than the conventions used in the PCMCIA specification and earlier versions of this specification. Signals are shown with their asserted state as High regardless of whether the signal is actually negative or positive true. Consequently, the –IORD, the -IOWR and the –IOCS16 signals are shown in the waveforms inverted from their electrical states on the bus.

Figure 8: True IDE PIO mode Read/Write waveforms



1. The device addresses consists of –CS0, –CS1, and A2–A0.
2. The Data I/O consist of D15–D0 (16–bit) or D7–D0 (8 bit).
3. –IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

Table 25: True IDE PIO mode Read/Write timing(1)

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)	5(5) (ns)	6(5) (ns)
Cycle time (min)	t_0(2)	600	383	240	180	120	100	80
Address Valid to –IORD/–IOWR setup (min)	t_1	70	50	30	30	25	15	10
–IORD/–IOWR (min)	t_2(2)	165	125	100	80	70	65	55
–IORD/–IOWR (min) Register (8 bit)	t_2(2)	290	290	290	80	70	65	55
–IORD/–IOWR recovery time (min)	t_{2i}(2)	–	–	–	70	25	25	20
–IOWR data setup (min)	t_3	60	45	30	30	20	20	15
–IOWR data hold (min)	t_4	30	20	15	10	10	5	5
–IORD data setup (min)	t_5	50	35	20	20	20	15	10
–IORD data hold (min)	t_{6z}(3)	5	5	5	5	5	5	5
–IORD data tri–state (max)	t_7(4)	30	30	30	30	30	20	20
Address valid to –IOCS16 assertion (max)	t_8(4)	90	50	40	NA	NA	NA	NA
Address valid to –IOCS16 released (max)	t_7	60	45	30	NA	NA	NA	NA
–IORD/–IOWR to address valid hold	t_9	20	15	10	10	10	10	10

1. The maximum load on –IOCS16 is 1 LSTTL with a 50pF total load.
2. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements of to, t_2, and t_{2i} have to be met. The requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can ensure that to is equal to or greater than the value reported in the devices identify drive Card implementation should support any legal host implementation.
3. This parameter specifies the time from the falling edge of –IORD to the moment when the CompactFlash Memory Card (tri–state).
4. t_7 and t_8 apply only to modes 0, 1 and 2. The –IOCS16 signal is not valid for other modes.

Figure 9: True IDE Multi-Word DMA Mode Read/Write waveforms

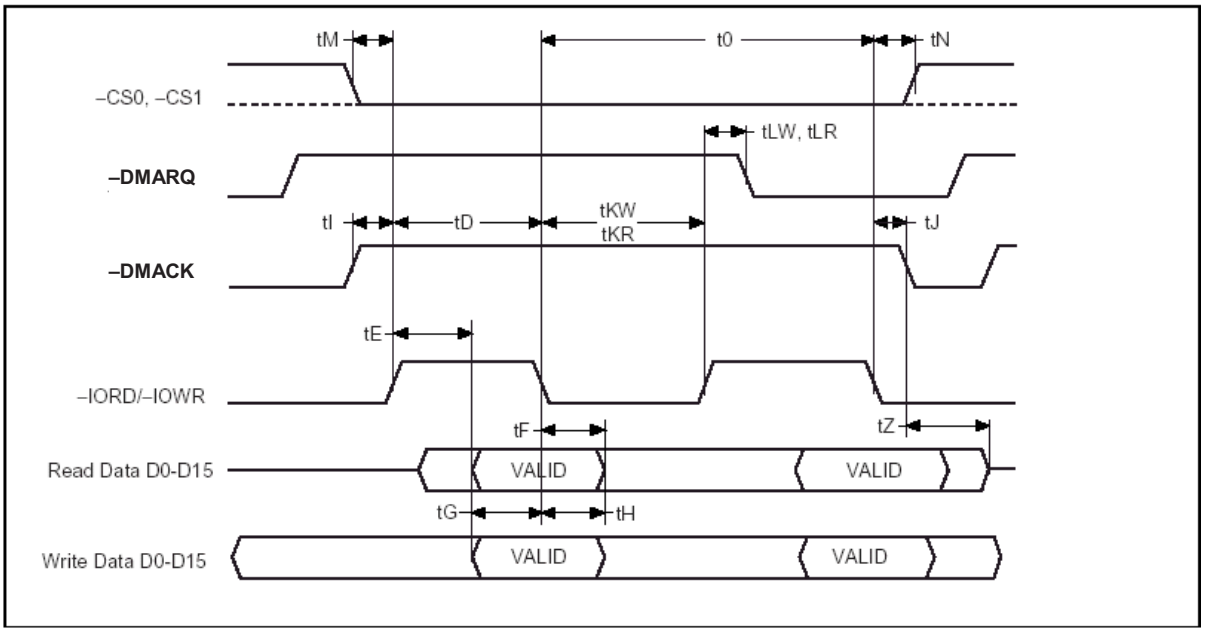


Table 26: True IDE Multi-Word DMA Mode Read/Write timing

Parameter	Symbol	Mode 0 (ns)	1 (ns)	2 (ns)	3 (ns)	4 (ns)
Cycle time (min)	t_0 (1)	480	150	120	100	80
-IORD / -IOWR asserted width (min)	t_D (1)	215	80	70	65	55
-IORD data access (max)	t_E	150	60	50	50	45
-IORD data hold (min)	t_F	5	5	5	5	5
-IORD/-IOWR data setup (min)	t_G	100	30	20	15	10
-IOWR data hold (min)	t_H	20	15	10	5	5
DMACK to –IORD/-IOWR setup (min)	t_I	0	0	0	0	0
-IORD / -IOWR to –DMACK hold (min)	t_J	20	5	5	5	5
-IORD Low width (min)	t_{KR} (1)	50	50	25	25	20
-IOWR Low width (min)	t_{KW} (1)	215	50	25	25	20
-IORD to DMARQ delay (max)	t_{LR}	120	40	35	35	35
-IOWR to DMARQ delay (max)	t_{LW}	40	40	35	35	35
CS(1:0) valid to –IORD / -IOWR	t_M	50	30	25	10	5
CS(1:0) hold	t_N	15	10	10	10	10
-DMACK	t_Z	20	25	25	25	25

1. t_0 is the minimum total cycle time. T_D is the minimum command active time. T_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles, respectively. The actual cycle time is the sum of the actual command active time and the actual command inactive time. The timing requirements of t_0, t_D, t_{KR}, and t_{KW} must be respected. T_0 is higher than $t_D + t_{KR}$ or $t_D + t_{KW}$, for input and output cycles respectively. This means the host can lengthen either t_D or t_{KR}/t_{KW}, or both, to ensure that t_o is equal to or higher than the value reported in the devices identify device data. A CompactFlash Storage Card implementation shall support any legal host implementation.

7 Card Configuration

The CompactFlash Memory Card is identified by information in the Card Information Structure (CIS). The Card has four configuration registers (Table 27and Table 28).

- Configuration Option Register
- Pin Replacement Register
- Card Configuration and Status Register
- Socket and Copy Register

They are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, in I/O Card mode these registers provide a method for accessing status information that would normally appear on dedicated pins in Memory Card mode.
The base address of the card configuration registers is 200h in the Attribute Memory space.
No write operation should be performed to the attribute memory area except for the configuration register addresses. All other attribute memory locations are reserved. See 7.5 *Attribute Memory Function.*

Table 27: CompactFlash Memory Card Registers and Memory Space Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Register Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D7 to D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D15 to D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit – D15 to D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Register Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7 to D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D15 to D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit – D15 to D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Write)

Table 28: CompactFlash Memory Card Configuration Registers Decoding

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8~A4	A3	A2	A1	A0	Selected Space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read(200h)
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write(200h)
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read (202h)
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write (202h)
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read (204h)
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write (204h)
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read (206h)
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write (206h)

Note: The location of the Card Configuration Registers should always be read from the CIS since these locations may vary in future products. No Writes should be performed to the Card Attribute Memory except to the Card Configuration Register Addresses. All other attribute memory locations are reserved.

7.1 Configuration Option Register (200h in Attribute Memory)

The Configuration Option Register is used to configure the Card's interface, address decoding and interrupt to the Card (see Table 29).

7.1.1 SRESET

Setting the SRESET bit to '1' and returning the bit '0' places the CompactFlash Storage Card in the Reset state. Setting this bit to '1' is equivalent to asserting the RESET signal except that the SRESET bit is not cleared. Returning the SRESET bit to '0' leaves the CompactFlash Storage Card in the same un-configured Reset state as after a power-up and hardware reset.
This bit is set to '0' at power-up and taking the Card through a hardware reset.

7.1.2 LevIREQ

This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) after Power Up.

7.1.3 Conf5 – Conf0 (Configuration Index)

These bits are used to select the operation mode of the Card as shown in Table 30. This bit is set to '0' after Power Up.

Table 29: Configuration Option Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

Table 30: CompactFlash Memory Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Mapping Mode	Card Mode	Task File Register Address
0	0	0	0	0	0	Memory	Memory	0h – Fh, 400h – 7FFh
0	0	0	0	0	1	Contiguous I/O	I/O	xx0h – xxFh
0	0	0	0	1	0	Primary I/O	I/O	1F0h – 1F7h, 3F6h – 3F7h
0	0	0	0	1	1	Secondary I/O	I/O	170h – 177h, 376h – 377h

7.2 CompactFlash Memory Card Configurations

The Card Configuration and Status Register contains information about the Card's status (see Table 31).

7.2.1 Changed

Indicates that one or both of the Pin Replacement register (CRDY, or CWProt) bits are set to '1'. When the Changed bit is set, -STSCHG (Pin 46) is held Low and if the SigChg bit is '1' the Card is configured for the I/O interface.

7.2.2 SigChg

This bit is set and reset by the host to enable and disable a state-change signal from the Status Register (issued on Status Changed pin 46). If no state change signal is desired, this bit should be set '0' and pin 46 (-STSCHG) will be held High while the Card is configured for I/O.

7.2.3 Iois8

The host sets this bit to '1' if the Card is to be configured in 8 bit I/O Mode. The Card is always configured for both 8 and 16 bit I/O, so this bit is ignored.

7.2.4 PwrDwn

This bit indicates whether the Card is in the power saving mode or active mode. When the PwrDwn bit is set to '1', the Card enters power down mode. When set to '0', the Card enters active mode. The READY value on Pin Replacement Register becomes BUSY when this bit is changed. READY will not become Ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.

7.2.5 Int

This bit represents the internal state of the interrupt request. It is available whether or not the I/O interface has been configured. It remains valid until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the –IEN bit in the Device Control Register, this bit is '0'.

Table 31: Card Configuration and Status Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOIS8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOIS8	0	0	PwrDwn	0	0

7.3 Pin Replacement Register (204h in Attribute Memory)

This register contains information on the state of the READY signal when configured in memory mode and the IREQ signal in I/O mode. See Table 32 and Table 33.

7.3.1 Cready

This bit is set to '1' when the bit Rready changes state. This bit can also be written by the host.

7.3.2 CWProt

This bit is set to '1' when the bit RWProt changes state. This bit can also be written by the host.

7.3.3 Rready

This bit is used to determine the internal state of the Ready signal. In I/O mode it is used as an interrupt request. When written, this bit acts as a mask (Mready) for writing the corresponding bit Cready.

7.3.4 Wprot

This bit is always '0' since the CompactFlash Memory Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding CWProt bit.

7.3.5 Mready

This bit acts as a mask for writing the corresponding Cready bit.

7.3.6 MWProt

This bit when written acts as a mask for writing the corresponding CWProt bit.

Table 32: Pin Replacement Register (default value: 0Ch)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	Cready	CWProt	1	1	Rready	Wprot
Write	0	0	Cready	CWProt	0	0	Rready	MWProt

Table 33: Pin Replacement Changed Bit/Mask Bit Values

Initial Value of 'C' Status	Written by Host		Final 'C' Bit	Comments
	'C' Bit	'M' Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

7.4 Socket and Copy Register (206h in Attribute Memory)

This register contains additional configuration information which identifies the Card from other cards. This register is always written by the system before writing the Configuration Option Register (see Table 34).

7.4.1 Drive

This value can be used to address two different cards in the case of twin card configuration.

7.4.2 X

The socket number is ignored by the Card.

Table 34: Socket and Copy Register (default value: 00h)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

7.5 Attribute Memory Function

Attribute memory is a space where identification and configuration information are stored. Only 8 bit wide accesses at even addresses can be performed in this area. The Card configuration registers are also located in the Attribute Memory area, at base address 200h. Attribute memory is not accessible in True IDE mode of operation.
For the Attribute Memory Read function, signals –REG and –OE must be active and –WE inactive during the cycle. As in the Main Memory Read functions, the signals –CE1 and –CE2 control the even and odd Byte address, but only the even Byte data is valid during the Attribute Memory access. Refer to Table 35 for signal states and bus validity.

Table 35: Attribute Memory Function

Function Mode	-REG	-CE2(1)	-CE1(1)	A10	A9	A0	-OE(1)	-WE(1)	D15 to D8	D7 to D0
Standby	X	H	H	X	X	X	X	X	High-Z	High-Z
Read Byte Access CIS (8 bits)	L	H	L	L	L	L	L	H	High-Z	Even Byte
Write Byte Access CIS (8 bits) Invalid	L	H	L	L	L	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	L	H	L	L	H	High-Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	L	H	L	H	L	Don't Care	Even Byte
Read Byte Access Configuration CF+ (8 bits)	L	H	L	X	X	L	L	H	High-Z	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) Invalid	L	L	L	L	L	X	H	L	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	L	H	X	H	L	Don't Care	Even Byte

- The –CE signal or both the –OE signal and the –WE signal must be de-asserted between consecutive cycle operations.

7.6 I/O Transfer Function

The I/O transfer to or from the Card can be either 8 or 16 bits. When a 16 bit accessible port is addressed, the –IOIS16 signal is asserted by the Card, otherwise it is de-asserted. When a 16 bit transfer is attempted, and the –IOIS16 signal is not asserted, the system must generate a pair of 8 bit references to access the Word's even and odd Bytes. The Card permits both 8 and 16 bit accesses to all of its I/O addresses, so –IOIS16 is asserted for all addresses (see Table 36).

Table 36: I/O Function

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L L	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Output Access (8 bits)	L L	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd Byte	Even Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd Byte	Even Byte
I/O Read Inhibit	H	X	X	X	L	H	Don't Care	Don't Care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd Byte	Don't Care

7.7 Common Memory Transfer Function

The Common Memory transfer to or from the Card permits both 8 or 16 bit access to all of the Common Memory addresses (see Table 37).

Table 37: Common Memory Function

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15 to D8	D7 to D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H H	H H	L L	L H	L L	H H	High Z High Z	Even Byte Odd Byte
Byte Write Access (8 bits)	H H	H H	L L	L H	H H	L L	Don't Care Don't Care	Even Byte Odd Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd Byte	Even Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd Byte	Don't Care

7.8 True IDE Mode I/O Function

The Card can be configured in a True IDE Mode of operation. It is configured in this mode only when the –OE signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data Register are

allowed. No Memory or Attribute Registers are accessible to the host. The Set Feature Command can be used to put the device in 8 bit Mode (see Table 38).
Removing and reinserting the Card while the host computer's power is on will reconfigure the Card to PC Card ATA mode.

Table 38: True IDE Mode I/O Function

Function Code	-CS1	-CS0	A2 to A0	-DMACK	-IORD	-IOWR	D15 to D8	D7 to D0
Invalid Mode	L	L	X	X	X	X	Undefined In/Out	Undefined In/Out
	L	X	X	L	L	X	Undefined Out	Undefined Out
	L	X	X	L	X	L	Undefined In	Undefined In
	X	L	X	L	L	X	Undefined Out	Undefined Out
	X	L	X	L	X	L	Undefined In	Undefined In
Standby Mode	H	H	X	H	X	X	High Z	High Z
Task File Write	H	L	1h-7h	H	H	L	Don't Care	Data In
Task File Read	H	L	1h-7h	H	L	H	High Z	Data Out
PIO Data Register Write	H	L	0	H	H	L	Odd-Byte In	Even-Byte In
DMA Data Register Write	H	L	X	L	H	L	Odd-Byte In	Even-Byte In
PIO Data Register Read	H	L	0	H	L	H	Odd-Byte Out	Even-Byte Out
DMA Data Register Read	H	H	X	L	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	H	L	Don't Care	Control In
Alternate Status Read	L	H	6h	H	L	H	High Z	Status Out
Drive Address	L	H	7h	H	L	H	High Z	Data Out

7.9 Host configuration requirements

The CompactFlash Advanced Timing modes include PCMCIA-style I/O modes that are faster than the original 250 ns cycle time (see *Section 4:* Product Specification).
Before configuring the Card interface for the I/O mode, the host must ensure that all the cards connected to a given electrical interface support I/O transfers faster than 250ns.
These modes must be used in the conditions described in *Section 0*. In particular, the host can be connected to one card only. Consequently, the host must not configure a card to operate in a CompactFlash Advanced Timing mode if two cards are sharing the same I/O lines in Master/Slave operation, or if it is connected to the card through a cable which length exceeds 0.15m.

8 Software interface

8.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash Memory Card can be configured as a high performance I/O device through:

- Standard PC-AT disk I/O address spaces
  - 1F0h-1F7h, 3F6h-3F7h (primary);
  - 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16 Byte I/O block using any available IRQ.
- Memory space.

Communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The PCMCIA interface connects peripherals to the host using four-register mapping methods. Table 39: I/O Configurations is a detailed description of these methods:

Table 39: I/O Configurations

Standards Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0h-Fh, 400h-7FFh	Memory Mapped
1	I/O	xx0h-xxFh	I/O Mapped 16 Continuous Registers
2	I/O	1F0-1F7h, 3F6h-3F7h	Primary I/O Mapped
3	I/O	170-177h, 376h-377h	Secondary I/O Mapped

8.2 Memory Mapped Addressing

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2Kbytes as shown in Table 40: Memory Mapped Decoding. This window accesses the Data Register FIFO. It does not allow random access to the data buffer within the Card.
Register 0 is accessed with −CE1 and −CE2 Low, as a Word register on the combined Odd and Even Data Bus (D15 to D0). It can also be accessed with −CE1 Low and −CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with −CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to address 0 with −CE1 High and −CE2 Low accesses the Error (read) or Feature (write) register.
Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even then odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.
Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 kByte memory window to the data register is provided so that hosts can perform memory-to-memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory-to-memory block move instruction. Some PCMCIA socket adapters also have embedded auto incrementing address logic.
A Word access to address at offset 8 will provide even data on the least significant Byte of the data bus, along with odd data at offset 9 on the most significant Byte of the data bus.

Table 40: Memory Mapped Decoding

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0
1	0	X	0	0	0	0	0h	Even Data Register	Even Data Register
1	0	X	0	0	0	1	1h	Error Register	Feature Register
1	0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
1	0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
1	0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
1	0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
1	0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
1	0	X	0	1	1	1	7h	Status Register	Command Register
1	0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
1	0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
1	0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register

-REG	A10	A9 to A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0
1	0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
1	0	X	1	1	1	1	Fh	Drive Address Register	Reserved
1	1	X	X	X	X	0	8h	Even Data Register	Even Data Register
1	1	X	X	X	X	1	9h	Odd Data Register	Odd Data Register

8.3 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the Card, the registers are accessed in the block of I/O space decoded by the system as shown in Table 41.
As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.
Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Register 8 is equivalent to register 0, while register 9 accesses the odd Byte. Therefore, if the registers are Byte accessed in the order 9 then 8 the data will be transferred odd Byte then even Byte. Repeated Byte accesses to register 8 or 0 will access consecutive (even than odd) Bytes from the data buffer. Repeated Word accesses to register 8, 9 or 0 will access consecutive Words from the data buffer, however repeated Byte accesses to register 9 are not supported. Repeated alternating Byte accesses to registers 8 then 9 will access consecutive (even then odd) Bytes from the data buffer.

Table 41: Contiguous I/O Decoding

-REG	A10 to A4	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0
0	X	0	0	0	0	0h	Even Data Register	Even Data Register
0	X	0	0	0	1	1h	Error Register	Feature Register
0	X	0	0	1	0	2h	Sector Count Register	Sector Count Register
0	X	0	0	1	1	3h	Sector Number Register	Sector Number Register
0	X	0	1	0	0	4h	Cylinder Low Register	Cylinder Low Register
0	X	0	1	0	1	5h	Cylinder High Register	Cylinder High Register
0	X	0	1	1	0	6h	Select Card/Head Register	Select Card/Head Register
0	X	0	1	1	1	7h	Status Register	Command Register
0	X	1	0	0	0	8h	Dup. Even Data Register	Dup. Even Data Register
0	X	1	0	0	1	9h	Dup. Odd Data Register	Dup. Odd Data Register
0	X	1	1	0	1	Dh	Dup. Error Register	Dup. Feature Register
0	X	1	1	1	0	Eh	Alternate Status Register	Device Control Register
0	X	1	1	1	1	Fh	Drive Address Register	Reserved

8.4 I/O Primary and Secondary Address Configurations

When the system decodes the Primary and Secondary Address Configurations, the registers are accessed in the block of I/O space as shown in Table 42.
As for the Memory Mapped Addressing, register 0 is accessed with –CE1 Low and –CE2 Low (and A0 don't Care) as a Word register on the combined Odd and Even Data Bus (D15 to D0). This register may also be accessed with –CE1 Low and –CE2 High, by a pair of Byte accesses to offset 0. The address space of this Word register overlaps the address space of the Error and Feature Byte-wide registers at offset 1. When accessed twice as Byte register with –CE1 Low, the first Byte is the even Byte of the Word and the second is the odd Byte. A Byte access to register 0 with –CE1 High and –CE2 Low accesses the error (read) or feature (write) register.

Table 42: Primary and Secondary I/O Decoding

-REG	A9 to A4	A3	A2	A1	A0	-IORD=0	-IOWR=0
0	1F(17)h	0	0	0	0	Even Data Register	Even Data Register
0	1F(17)h	0	0	0	1	Error Register	Feature Register
0	1F(17)h	0	0	1	0	Sector Count Register	Sector Count Register
0	1F(17)h	0	0	1	1	Sector Number Register	Sector Number Register
0	1F(17)h	0	1	0	0	Cylinder Low Register	Cylinder Low Register
0	1F(17)h	0	1	0	1	Cylinder High Register	Cylinder High Register
0	1F(17)h	0	1	1	0	Select Card/Head Register	Select Card/Head Register
0	1F(17)h	0	1	1	1	Status Register	Command Register
0	3F(37)h	0	1	1	0	Alternate Status Register	Device Control Register
0	3F(37)h	0	1	1	1	Drive Address Register	Reserved

8.5 True IDE Mode Addressing

When the Card is configured in the True IDE Mode, the I/O decoding is as shown in Table 43.

Table 43: True IDE Mode I/O Decoding

-CS1	-CS0	A2	A1	A0	-DMACK	-IORD=0	-IOWR=0
1	0	0	0	0	1	PIO RD Data	PIO WR Data
1	1	X	X	X	0	DMA RD Data	DMA WR Data
1	0	0	0	1	1	Error Register	Features
1	0	0	1	0	1	Sector Count	Sector Count
1	0	0	1	1	1	Sector No.	Sector No.
1	0	1	0	0	1	Cylinder Low	Cylinder Low
1	0	1	0	1	1	Cylinder High	Cylinder High
1	0	1	1	0	1	Select Card/Head	Select Card/Head
1	0	1	1	1	1	Status	Command
0	1	1	1	0	1	Alt Status	Alt Status

9 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the Card. These registers are collectively referred to as the 'task file'.
In accordance with the PCMCIA specification, each register that is located at an odd offset address can be accessed in the PC Card Memory or PC Card I/O modes. The register can be addressed in two ways:

- Using the normal register address.
- Using the corresponding even address (normal address -1) when –CE1 is High and –CE2 Low, unless –IOIS16 is High (not asserted by the card) and an I/O cycle is in progress. Register data are input or output on data bus lines D15-D8.

In True IDE mode, the size of the transfer is based solely on the register being addressed. All registers are 8-bit only except for the Data Register, which is normally 16 bits. However, they can be configured to be accessed in 8-bit mode for non-DMA operations, by using a Set Features command (see *Section 10.17*).

9.1 Data Register

The Data register is located at address 1F0h [170h], offset 0h, 8h, and 9h.
The Data Register is a 16 bit register used to transfer data blocks between the Card data buffer and the Host. This register overlaps the Error Register. Table 44 and Table 45 describe the combinations of Data register access and explain the overlapped Data and Error/Feature Registers. Because of the overlapped registers, access to the 1F1h, 171h or offset 1 are not defined for Word (-CE2 and –CE1 set to '0') operations, and are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed.

Table 44: Data Register Access (Memory and I/O mode)

Data Register	-CE2	-CE1	A0	-REG*	Offset	Data Bus
Word Data Register	0	0	X	-	0h, 8h, 9h	D15 to D0
Even Data Register	1	0	0	-	0h, 8h	D7 to D0
Odd Data Register	1	0	1	-	9h	D7 to D0
Odd Data Register	0	1	X	-	8h, 9h	D15 to D8
Error/Feature Register	1	0	1	-	1h, Dh	D7 to D0
Error/Feature Register	0	1	X	-	1h	D15 to D8
Error/Feature Register	0	0	X	-	Dh	D15 to D8

- –REG signal is mode dependent. It must be Low when the Card operates in I/O Mode and High when it operates in Memory Mode.

Table 45: Data Register Access (True IDE mode)

Data Register	-CS1	-CS0	A0	-DMACK	Offset	Data Bus
PIO Word Data Register	1	0	0	1	0h	D15 to D0
DMA Word Data Register	1	1	X	0	X	D15 to D0
PIO Byte Data Register (Selected Using Set Features Command)	1	0	0	1	0h	D7 to D0

9.2 Error Register

The Error register is a read-only register, located at address 1F1h [171h], offset 1h, 0Dh.
This read only register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined in Table 46 This register is accessed on data bits D15 to D8 during a write operation to offset 0 with –CE2 Low and –CE1 High.

9.2.1 Bit 7 (BBK)

This bit is set when a Bad Block is detected.

9.2.2 Bit 6 (UNC)

This bit is set when an Uncorrectable Error is encountered.

9.2.3 Bit 5

This bit is '0'.

9.2.4 Bit 4 (IDNF)

This bit is set if the requested sector ID is in error or cannot be found.

9.2.5 Bit 3

This bit is '0'.

9.2.6 Bit 2 (Abort)

This bit is set if the command has been aborted because of a Card status condition (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

9.2.7 Bit 1

This bit is '0'.

9.2.8 Bit 0 (AMNF)

This bit is set when there is a general error.

Table 46: Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

9.3 Feature Register

The Feature register is a write-only register, located at address 1F1h [171h], offset 1h, Dh.
This write-only register provides information on features that the host can utilize. It is accessed on data bits D15 to D8 during a write operation to Offset 0 with –CE2 Low and –CE1 High.

9.4 Sector Count Register

The Sector Count register is located at address 1F2h [172h], offset 2h.
This register contains the number of sectors of data to be transferred on a read or write operation between the host and Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request. The default value is 01h.

9.5 Sector Number (LBA 7-0) Register

The Sector Number register is located at address 1F3h [173h], offset 3h.
This register contains the starting sector number or bits 7 to 0 of the Logical Block Address (LBA), for any data access for the subsequent sector transfer command.

9.6 Cylinder Low (LBA 15-8) Register

The Cylinder Low register is located at address 1F4h [174h], offset 4h.
This register contains the least significant 8 bits of the starting cylinder address or bits 15 to 8 of the Logical Block Address.

9.7 Cylinder High (LBA 23-16) Register

The Cylinder High register is located at address 1F5h [175h], offset 5h.
This register contains the most significant bits of the starting cylinder address or bits 23 to 16 of the Logical Block Address.

9.8 Drive/Head (LBA 27-24) Register

The Driver/Head register is located at address 1F6h [176h], offset 6h.
The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined in Table 47.

9.8.1 Bit 7

This bit is set to '1'.

9.8.2 Bit 6 (LBA)

LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA is set to '0', Cylinder/Head/Sector mode is selected. When LBA is set to'1', Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

- LBA7-LBA0: Sector Number Register D7 to D0
- LBA15-LBA8: Cylinder Low Register D7 to D0
- LBA23-LBA16: Cylinder High Register D7 to D0
- LBA27-LBA24: Drive/Head Register bits HS3 to HS0

9.8.3 Bit 5

This bit is set to '1'.

9.8.4 Bit 4 (DRV)

DRV is the drive number. When DRV is '0', drive/card 0 is selected (Master). When DRV is '1', drive/card 1 is selected (Slave). The Card is set to Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.

9.8.5 Bit 3 (HS3)

When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is bit 27 in the Logical Block Address mode.

9.8.6 Bit 2 (HS2)

When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is bit 26 in the Logical Block Address mode.

9.8.7 Bit 1 (HS1)

When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

9.8.8 Bit 0 (HS0)

When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Table 47: Drive/Head Register

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

9.9 Status & Alternate Status Registers

The Status & Alternate Status registers are located at addresses 1F7h [177h] and 3F6h [376h], respectively. Offsets are 7h and Eh.
These registers return the Card status when read by the host.
Reading the Status Register clears a pending interrupt. Reading the Auxiliary Status Register does not clear a pending interrupt.
The Status Register should be accessed in Byte mode; in Word mode it is recommended that Alternate Status Register is used. The status bits are described as follows

9.9.1 Bit 7 (BUSY)

The busy bit is set when only the Card can access the command register and buffer, The host is denied access. No other bits in this register are valid when this bit is set to '1'.

9.9.2 Bit 6 (RDY)

This bit indicates whether the device is capable of performing CompactFlash Memory Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.

9.9.3 Bit 5 (DWF)

When set this bit indicates a Write Fault has occurred.

9.9.4 Bit 4 (DSC)

This bit is set when the Card is ready.

9.9.5 Bit 3 (DRQ)

The Data Request is set when the Card requires information be transferred either to or from the host through the Data register. The bit is cleared by the next command.

9.9.6 Bit 2 (CORR)

This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

9.9.7 Bit 1 (IDX)

This bit is always set to '0'.

9.9.8 Bit 0 (ERR)

This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. In case of read or write access commands that end with an error, the address of the first sector with an error is in the command block registers. This bit is cleared by the next command.

Table 48: Status & Alternate Status Register

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

9.10 Device Control Register

The Device Control register is located at address 3F6h [376h], offset Eh.
This Write-only register is used to control the CompactFlash Memory Card interrupt request and to issue an ATA soft reset to the Card. This register can be written even if the device is BUSY. The bits are defined as follows:

9.10.1 Bit 7 to 3

Don't care. The host should reset this bit to '0'.

9.10.2 Bit 2 (SW Rst)

This bit is set to 1 in order to force the CompactFlash Storage Card to perform an AT Disk controller Soft Reset operation. This clears Status Register and writes Diagnostic Code in Error register after a Write or Read Sector error. The Card remains in Reset until this bit is reset to '0.'

9.10.3 Bit 1 (-Ien)

When the Interrupt Enable bit is set to '0', -IREQ interrupts are enabled. When the bit is set to '1', interrupts from the Card are disabled. This bit also controls the Int bit in the Card Configuration and Status Register. It is set to '0' at Power On.

9.10.4 Bit 0

This bit is set to '0'.

Table 49: Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X(0)	X(0)	X(0)	X(0)	X(0)	SW Rst	-Ien	0

9.11 Card (Drive) Address Register

The Card (Drive) Address register is located at address 3F7h [377h], offset Fh.
This read-only register is provided for compatibility with the AT disk drive interface and can be used for confirming the drive status. It is recommended that this register is not mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

9.11.1 Bit 7

This bit is don't care.

9.11.2 Bit 6 (-WTG)

This bit is '0' when a write operation is in progress; otherwise, it is '1'.

9.11.3 Bit 5 (-HS3)

This bit is the negation of bit 3 in the Drive/Head register.

9.11.4 Bit 4 (-HS2)

This bit is the negation of bit 2 in the Drive/Head register.

9.11.5 Bit 3 (-HS1)

This bit is the negation of bit 1 in the Drive/Head register.

9.11.6 Bit 2 (-HS0)

This bit is the negation of bit 0 in the Drive/Head register.

9.11.7 Bit 1 (-nDS1)

This bit is '0' when drive 1 is active and selected.

9.11.8 Bit 0 (-nDS0)

This bit is '0' when the drive 0 is active and selected.

Table 50: Card (Drive) Address Register

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

10 CF-ATA command description

This section defines the software requirements and the format of the commands the Host sends to the Card. Commands are issued to the Card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command Register. There are three classes of command acceptance, all dependent on the host not issuing commands unless the Card is not busy (BSY is '0').

- **Class 1:** Upon receipt of a Class 1 command, the Card sets BSY within 400ns.
- **Class 2:** Upon receipt of a Class 2 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 700µs, and clears BSY within 400ns of setting DRQ.
- **Class 3:**Upon receipt of a Class 3 command, the Card sets BSY within 400ns, sets up the sector buffer for a write operation, sets DRQ within 20ms (assuming no re-assignments), and clears BSY within 400ns of setting DRQ.

For reasons of backward compatibility some commands are implemented as 'no operation' NOP.
Table 51 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Table 51: CF-ATA Command Set[1]

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	E5h or 98h					D	
1	Execute Drive Diagnostic	90h					YD	
1	Erase Sector(s)	C0h		Y	Y	Y	Y	Y
1	Identify Drive	Ech					D	
1	Idle	E3h or 97h		Y			D	
1	Idle Immediate	E1h or 95h					D	
1	Initialize Drive Parameters	91h		Y			Y	
1	NOP	00h					D	
1	Read Buffer	E4h					D	
1	Read DMA	C8		Y	Y	Y	Y	Y
1	Read Multiple	C4h		Y	Y	Y	Y	Y
1	Read Sector(s)	20h or 21h		Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40h or 41h		Y	Y	Y	Y	Y
1	Recalibrate	1Xh					D	
1	Request Sense	03h					D	
1	Seek	7Xh			Y	Y	Y	Y
1	Set Features	Efh	Y				D	
1	Set Multiple Mode	C6h		Y			D	
1	Set Sleep Mode	E6h or 99h					D	
1	Stand By	E2h or 96h					D	
1	Stand By Immediate	E0h or 94h					D	
1	Translate Sector	87h		Y	Y	Y	Y	Y
1	Wear Level	F5h					Y	
2	Write Buffer	E8h					D	
2	Write DMA	CA		Y	Y	Y	Y	Y
3	Write Multiple	C5h		Y	Y	Y	Y	Y
3	Write Multiple w/o Erase	CDh		Y	Y	Y	Y	Y
2	Write Sector(s)	30h or 31h		Y	Y	Y	Y	Y
2	Write Sector(s) w/o Erase	38h		Y	Y	Y	Y	Y
3	Write Verify	3Ch		Y	Y	Y	Y	Y

1. FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Card/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use), Y – The register contains a valid parameter for this command. For the Drive/Head Register Y means both the CompactFlash Memory Card and head parameters are used. D – only the Compact Flash Memory Card parameter is valid and not the head parameter C – the register contains command specific data (see command descriptors for use).

10.1 Check Power Mode (98h or E5h)

This command checks the power mode.
Issuing the command while the Card is in Standby mode, is about to enter Standby, or is exiting Standby, the command will set BSY, set the Sector Count Register to 00h, clear BSY and generate an interrupt.
Issuing the command when the Card is in Idle mode will set BSY, set the Sector Count Register to FFh, clear BSY and generate an interrupt.
Table 52 defines the Byte sequence of the Check Power Mode command.

Table 52: Check Power Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h or E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.2 Execute Drive Diagnostic (90h)

This command performs the internal diagnostic tests implemented by the Card.
In PCMCIA configuration, this command only runs on the Card which is addressed by the Drive/Head register when the command is issued. This is because PCMCIA Card interface does not allow for direct inter-drive communication.
In True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with the status for both devices.
Table 53 defines the Execute Drive Diagnostic command Byte sequence. The Diagnostic codes shown in Table 54 are returned in the Error Register at the end of the command.

Table 53: Execute Drive Diagnostic

Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 54: Diagnostic Codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error in True IDE Mode

10.3 Erase Sector(s) (C0h)

This command is used to pre-erase and condition data sectors prior to a Write Sector without Erase command or a Write Multiple Without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur. Table 55 defines the Byte sequence of the Erase Sector command.

Table 55: Erase Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to erase							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to erase							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

10.4 Identify Drive (Ech)

The Identify Drive command enables the host to receive parameter information from the Card. This command has the same protocol as the Read Sector(s) command. Table 56 defines the Identify Drive

command Byte sequence. All reserved bits or Words are zero. Table 57 shows the definition of each field in the Identify Drive Information.

10.4.1 Word 0: General Configuration

This field indicates the general characteristics of the device.
The default value for Word 0 is set to **848Ah**. It is recommended that PCMCIA modes of operation report only the 848Ah value as they are always intended as removable devices.
Alternate Configuration Values for Word 0 is **044Ah**.
Some operating systems require Bit 6 of Word 0 to be set to '1' (Non-removable device) to use the Card as the root storage device. The Card must be the root storage device when a host completely replaces conventional disk storage with a CompactFlash Card in True IDE mode. To support this requirement and provide capability for any future removable media cards, alternate value of Word 0 is set in True IDE Mode of operation.

10.4.2 Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

10.4.3 Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

10.4.4 Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

10.4.5 Word 7-8: Number of Sectors per Card

This field contains the number of sectors per Card. This double Word value is also the first invalid address in LBA translation mode.

10.4.6 Word 10-19: Memory Card Serial Number

The contents of this field are right justified and padded without spaces (20h).

10.4.7 Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

10.4.8 Word 27-46: Model Number

This field contains the model number for this product and is left justified and padded with spaces (20h).

10.4.9 Word 47: Read/Write Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands.

10.4.10 Word 49: Capabilities

- Bit 13 Standby Timer: is set to '0' to indicate that the Standby timer operation is defined by the manufacturer.
- Bit 9 LBA support: CompactFlash Memory Cards support LBA mode addressing.
- Bit 8 DMA Support: Read/Write DMA commands are supported.

10.4.11 Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. For backward compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51, the highest original PIO mode it can support (PIO mode 0, 1 or 2). Bits 15-8: are set to 02H.

10.4.12 Word 53: Translation Parameter Valid

- Bit 1: is set to '1' to indicate that Words 64 to 70 are valid
- Bit 0: is set to '1' to indicate that Words 54 to 58 are valid

10.4.13 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

10.4.14 Word 57-58: Current Capacity

This field contains the product of the current cylinders, heads and sectors.

10.4.15 Word 59: Multiple Sector Setting

- Bits 15-9 are reserved and must be set to '0'.
- Bit 8 is set to '1', to indicate that the Multiple Sector Setting is valid.
- Bits 7-0 are the current setting for the number of sectors to be transferred for every interrupt, on Read/Write Multiple commands; the only values returned are '00h' or '01h'.

10.4.16 Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the Card in LBA mode only.

10.4.17 Word 63: Multi-Word DMA transfer

Bits 15 through 8 of Word 63 of the Identify Device parameter information identifies which Multi-Word DMA mode that has been selected by host. Each bit of Word 0 is significant. Only one of these bits can be set to '1' by the CompactFlash Storage Card to indicate the Multi-Word DMA mode which is currently selected:

- Bits 15 to 11 are reserved.
- Bit 10: when set to '1', it indicates that Multi-Word DMA mode 1 has been selected.
- Bit 9: when set to '1', it indicates that Multi-Word DMA mode 1 has been selected.
- Bit 8: when set to '1', it indicates that Multi-Word DMA mode 0 has been selected.

Bits 7 to 0 define the Multi-Word DMA data transfer supported field. Any number of bits may be set to one in this field by the CompactFlash Storage Card to indicate which Multi-Word DMA mode is supported:

- Bit 7 to 3 are reserved.
- Bit 2: when set to '1', it indicates that the CompactFlash Storage Card supports Multi-Word DMA modes 2, 1 and 0.
- Bit 1: when set to '1', it indicates that the CompactFlash Storage Card supports Multi-Word DMA modes 1 and 0.
- Bit 0: when set to '1', it indicates that the CompactFlash Storage Card supports Multi-Word DMA mode 0.

Note: 1 Selection of Multi-Word DMA modes 3 and above are specific to CompactFlash, and are reported in Word 163.
2 Support for Multi-Word DMA modes 3 and above are specific to CompactFlash are reported in Word 163.

10.4.18 Word 64: Advanced PIO transfer modes supported

This field is bit significant. Any number of bits may be set to '1' in this field by the CompactFlash Memory Card to indicate the advanced PIO modes it is capable of supporting.

- Bits 7-2 are reserved for future advanced PIO modes.
- Bit 1 is set to '1', indicates that the CompactFlash Memory Card supports PIO mode 4.
- Bit 0 is set to '1' to indicate that the CompactFlash Memory Card supports PIO mode 3.

Note: Support for PIO modes 5 and above is specific to CompactFlash are reported in Word 163

10.4.19 Word 65: Minimum Multi-Word DMA transfer cycle time

Word 65 of the parameter information of the Identify Device command is defined as the minimum Multi-Word DMA transfer cycle time.
It corresponds to the minimum cycle time for which the Card ensures data integrity during transfers. It is expressed in nanoseconds.
The returned value is '50h' (for Cycle time values refer to Table 25).

10.4.20 Word 66: Recommended Multi-Word DMA transfer cycle time

Word 66 of the parameter information of the Identify Device command is defined as the recommended Multi-Word DMA transfer cycle time. The returned value is '50h' (for Cycle time values refer to *Table 22*).

10.4.21 Word 67: Minimum PIO transfer cycle time without flow control

This field gives the minimum cycle time (in ns) that the host should use for the

CompactFlash Memory Card to ensure data integrity during transfers when flow control is not used. The returned value is '50h' (for Cycle time values refer to Table 25).

10.4.22 Word 68: Minimum PIO transfer cycle time with IORDY

This field gives the minimum cycle time (in ns) supported by the CompactFlash Memory Card to perform data transfers using IORDY flow control. The returned value is '50h' (for Cycle time values refer to Table 25).

10.4.23 Word 163: Advanced True IDE Timing mode capabilities and settings

This word describes the capabilities and current settings for CFA defined Advanced Timing modes using the True IDE interface.
There are four sub-fields that describe the Advanced PIO and Advanced Multi-Word DMA Timing modes supported and selected:

- Bits 2-0: Advanced True IDE PIO Mode supported.
  The returned value is '2h' to indicate that PIO mode 6 is the highest PIO mode supported.
- Bits 5-3: Advanced True IDE Multi-Word DMA mode supported.
  The returned value is '2h' to indicate that Multi-Word DMA mode 4 is the highest Multi-Word DMA mode supported.
- Bits 8-6: Advanced True IDE PIO mode selected.
  These bits indicate the current True IDE PIO mode selected on the Card.
- Bits 11-9: Advanced True IDE Multi-Word DMA mode selected.
  These bits indicate the current True IDE Multi-Word DMA mode selected on the Card.

10.4.24 Word 164: Advanced PCMCIA I/O and Memory Timing modes capabilities and settings

This Word describes the capabilities and current settings for CFA defined Advanced Timing modes using the Memory and PCMCIA I/O interface:

- Bits 2-0: maximum Advanced PCMCIA I/O mode supported.
  The returned value is '3h' to indicate that 80ns is the maximum I/O timing mode supported by the Card.
- Bits 5-3: maximum PCMCIA Memory timing mode supported.
  The returned value is '3h' to indicate that 80ns is the maximum PCMCIA Memory timing mode supported by the Card.

Table 56: Identify Drive

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Ech							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 57: Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848Ah*	2	General Configuration (signature of the CompactFlash Memory Card) REMOVABLE – Standard in PCMCIA mode
	045Ah*	2	Alternate Configuration. FIX – Standard in True IDE mode
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per Card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	aaaa	20	Serial number in ASCII (right justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Reserved

Word Address	Default Value	Total Bytes	Data Field Type Information
23-26	aaaa	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	aaaa	40	Model number in ASCII (right justified) Big Endian Byte Order in Word (COMPACTFLASH Hix)
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	**0300h** **0200h**	2	Capabilities with DMA without DMA
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0003h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved.
63	0407h* 0000h*	2	Multi-Word DMA transfer. In PCMCIA mode, this value is 'oh'.
64	0003h	2	Advanced PIO modes supported
65	**0078h*** **0000h***	2	Minimum Multi-Word DMA transfer cycle time per Word. In PCMCIA mode this value is 'oh'.
66	**0078h*** **0000h***	2	Recommended Multi-Word DMA transfer cycle time. In PCMCIA mode this value is 'oh'.
67	**0078h***	2	Minimum PIO transfer cycle time without flow control
68	**0078h***	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000h	20	Reserved
80-81	0000h	4	Reserved – CF cards do not return an ATA version
82-84	0000h	6	Features/command sets supported
85-87	0000h	6	Features/command sets enabled
88	0000h	2	Ultra DMA Mode Supported and Selected
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power management value
92-127	0000h	72	Reserved
128	0000h	2	Security status
129-159	0000h	64	vendor unique bytes
160	0000h	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	0492h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	001Bh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability
165-175	0000h	22	Reserved for assignment by the CFA
176-255	0000h	140	Reserved

- standard values (could be different in different configurations)
- XXXX Depending on Card density and drive geometry

10.5 Idle (97h or E3h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count (each count is 5ms) and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5ms) is different from the ATA specification.

Table 58 defines the Byte sequence of the Idle command.

Table 58: Idle

Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h or E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Timer Count (5ms increments)							
FEATURES	nu							

10.6 Idle Immediate (95h or E1h)

This command causes the Card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. Table 59 defines the Idle Immediate command Byte sequence.

Table 59: Idle Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h or E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.7 Initialize Drive Parameters (91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Drive/Head registers are used by this command. Table 60 defines the Initialize Drive Parameters command Byte sequence.

Table 60: Initialize Drive Parameters

Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Number of Sectors per Track							
FEATURES	nu							

10.8 NOP (00h)

This command always fails with the CompactFlash Memory Card returning command aborted. Table 61 defines the Byte sequence of the NOP command.

Table 61: NOP

Task File Register	7	6	5	4	3	2	1	0
COMMAND	00h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.9 Read Buffer (E4h)

The Read Buffer command enables the host to read the current contents of the Card's sector buffer. This command has the same protocol as the Read Sector(s) command. Table 62 defines the Read Buffer command Byte sequence.

Table 62: Read buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.10 Read DMA (C8h)

This command uses Multi-Word DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. If the sector count is set to '0', 256 sectors will be read by issuing a Read DMA command.
Data transfer begins at the sector specified in the Sector Number Register. When the Read DMA command is issued, the CompactFlash Card asserts BSY, and transfers all or part of the sector data in the buffer. The Card can then set DRQ and clear BSY, although it is not required.
The Card asserts DMARQ when data are available to be transferred. The host then reads the 512*sector-count Bytes of data from the Card using DMA protocol. When DMARQ is asserted, the host asserts –DMACK to notify it is ready to transfer data, and asserts –IORD once for each 16 bit Word to be transferred.
Interrupts are not generated for each sector transfer, but when all sectors have been transferred or when an error occurred during the operation.
An Abort error is returned by the Card when a Read DMA command is sent by the host and the 8-bit transfer mode has been enabled by the Set Features command.
Table 63 defines the Read DMA command Byte sequence.

Table 63: Read DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.11 Read Multiple (C4h)

The Read Multiple command performs similarly to the Read Sectors command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.
Command execution is identical to the Read Sectors operation except that the number of sectors defined by a Set Multiple command is transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.
The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Read Multiple command. When the Read Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Read Multiple command is attempted before the Set Multiple Mode command has been executed or when Read Multiple commands are disabled, the Read Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read Sector(s) Command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer.
Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.
Table 64 defines the Read Multiple command Byte sequence.

Table 64: Read Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C4h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.12 Read Sector(s) (20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has been read by the host, the Card sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.
If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data are pending in the sector buffer. Table 65 defines the Read Sector command Byte sequence.

Table 65: Read sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h or 21h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.13 Read Verify Sector(s) (40h or 41h)

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the Card sets BSY. When the requested sectors have been verified, the Card clears BSY and generates an interrupt.
If an error occurs, the verify terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.
Table 66 defines the Read Verify Sector command Byte sequence.

Table 66: Read Verify Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h or 41h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector Number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.14 Recalibrate (1Xh)

This command is effectively a NOP command to the Card and is provided for compatibility purposes. Table 67 defines the Recalibrate command Byte sequence.

Table 67: Recalibrate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	1Xh							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.15 Request Sense (03h)

This command requests extended error information for the previous command. Table 68 defines the Request Sense command Byte sequence. Table 69 defines the valid extended error codes. The extended error code is returned to the host in the Error Register.

Table 68: Request sense

Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	1	LBA	1	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Table 69: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK (No Error)
09h	Miscellaneous Error
21h	Invalid Address (Requested Head or Sector Invalid)
2Fh	Address Overflow (Address Too Large)
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrectable ECC Error
18h	Corrected ECC Error
05h, 30-34h, 37h, 3Eh	Self Test or Diagnostic Failed
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error / Aborted Command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted Media Format
03h	Write / Erase Failed

10.16 Seek (7Xh)

This command is effectively a NOP command to the Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range. Table 70 shows the Seek command Byte sequence.

Table 70: Seek

Task File Register	7	6	5	4	3	2	1	0
COMMAND	7Xh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

10.17 Set Features (Efh)

This command is used by the host to establish or select certain features. Table 71 shows the Set Features command Byte sequence. Table 72 defines all features that are supported.

- Features 01h and 81h are used to enable and clear 8 bit data transfer modes in True IDE Mode. If the 01h feature command is issued all data transfers will occur on the D7-D0 data lines and the –IOIS16 signal will not be asserted for data register accesses. The host must not enable this feature for DMA transfers.
- Feature 03h allows the host to select the PIO or the Multi-Word DMA transfer mode. The number of sectors to be transferred must be specified in the Sector Count register (see Table 73 for values). The upper 5 bits define the type of transfer and the lower 3 bits encode the transfer mode. Only one PIO mode and one Multi-Word mode can be selected at a time. The host can change the selected mode by issuing the Set Features command.
- Feature code 9Ah allows the host to configure the Card to best meet the host system power requirements. The host programs the Sector Count register to a value that is equal to one-fourth of the desired maximum average current (in mA) that the Card should consume. For example, if the Sector Count register is set to '6', the Card must be configured to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the Card replies to the host with the range of values that it supports. The minimum value is set in the Cylinder Low Register, and the maximum value is set in the Cylinder Hi register. After power-up, the Card defaults to operate at the highest performance and therefore in the highest current mode. Values outside this programmable range are accepted by the card. However, the Card will operate either at the lowest power or highest performance as appropriate.

Table 71: Set Features

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Efh							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Config							
FEATURES	Feature							

Table 72: Features Supported

Feature	Operation
01h	Enable 8-bit data transfers.
03h	Set transfer mode based on value in Sector Count register.
55h	Disable Read Look Ahead.
69h	NOP Accepted for backward compatibility.
81h	Disable 8 bit data transfer.
96h	NOP Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
9Ah	Set the host current source capability. Allows trade-off between current drawn and read/write speed.

Table 73: Transfer Mode Values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode(1)
Reserved	00010b	N/A
Multi-Word DMA mode	00100b	Mode

- Mode = transfer mode number

10.18 Set Multiple Mode (C6h)

This command enables the Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the Card sets BSY and checks the Sector Count Register.
If the Sector Count Register contains a valid value and the block count is supported, the value is loaded for all subsequent Read Multiple and Write Multiple commands and execution is enabled. If a block count is

not supported, an Aborted Command error is posted, and Read Multiple and Write Multiple commands are disabled. If the Sector Count Register contains '0' when the command is issued, Read and Write Multiple commands are disabled. At power on the default mode is Read and Write Multiple disabled, unless it is disabled by a Set Feature command. Table 74 defines the Set Multiple Mode command Byte sequence.

Table 74: Set Multiple Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.19 Set Sleep Mode (99h or E6h)

This command causes the CompactFlash Memory Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command. Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds. Note that this time base (5ms) is different from the ATA Specification. Table 75 defines the Set Sleep Mode command Byte sequence.

Table 75: Set Sleep Mode

Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h or E6h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.20 Standby (96h or E2)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA 'Standby' Mode), clear BSY and return the interrupt immediately. Recovery from Sleep mode is accomplished by issuing another command. Table 76 defines the Standby command Byte sequence.

Table 76: Standby

Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h or E2h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.21 Standby Immediate (94h or E0h)

This command causes the Card to set BSY, enter the Sleep mode (which corresponds to the ATA Standby Mode), clear BSY and return the interrupt immediately.
Recovery from Sleep mode is accomplished by issuing another command.

Table 77 defines the Standby Immediate Byte sequence.

Table 77: Standby Immediate

Task File Register	7	6	5	4	3	2	1	0
COMMAND	94h or E0h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.22 Translate Sector (87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head and sector, including its Logical Address, and the Hot Count, if available, for that sector. Table 78defines the Translate Sector command Byte sequence. Table 79 represents the information in the buffer.

Table 78: Translate Sector

Task File Register	7	6	5	4	3	2	1	0
COMMAND	87h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	nu (LBA7-0)							
SECTOR COUNT	nu							
FEATURES	nu							

Table 79: Translate sector Information

Address	Information
00h-01h	Cylinder MSB (00), Cylinder LSB (01)
02h	Head
03h	Sector
04-06h	LBA MSB (04) – LSB (06)
07-12h	Reserved
13h	Erased Flag (FFh) = Erased; 00h = Not Erased
14h-17h	Reserved
18h-1Ah	Hot Count MSB (18) – LSB (1A); 0 = Hot Count not supported
1Bh-1FFh	Reserved

10.23 Wear Level (F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with a '00h' indicating Wear Level is not needed.
Table 80 defines the Wear Level command Byte sequence.

Table 80: Wear level

Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Completion Status							
FEATURES	nu							

10.24 Write Buffer (E8h)

The Write Buffer command enables the host to overwrite contents of the Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 Bytes.
Table 81 defines the Write Buffer command Byte sequence.

Table 81: Write Buffer

Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu			D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

10.25 Write DMA (Cah)

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. If the sector count is set to '0', 256 sectors will be read by issuing a Read DMA command.
The transfer begins at the sector specified in the Sector Number Register. When the Write DAM command is issued, the CompactFlash Storage Card asserts BSY and transfers all or part of the sector data in the buffer. The Card can then set DRQ and clear BSY, although it is not required.
The Card asserts DMARQ when data are available to be transferred. The host then writes the 512*sector-count Bytes of data to the Card using the DMA protocol. When DMARQ is asserted by the Card, the host asserts –DMACK to notify that it is ready to transfer data, and asserts –IOWR once for each 16 bit Word to be transferred.
Interrupts are not generated for each sector transfer, but when all sectors have been transferred or when an error occurred during the operation.
An Abort error is returned by the Card when a Write DMA command is sent by the host and the 8-bit transfer mode has been enabled by the Set Features command.
Table 82 defines the Write DMA command Byte sequence.

Table 82: Write DMA

Task File Register	7	6	5	4	3	2	1	0
COMMAND	Cah							
DRIVE/HEAD	LBA			D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.26 Write Multiple Command (C5h)

This command is similar to the Write Sectors command. The Card sets BSY within 400ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.
DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set Multiple Mode command, which must be executed prior to the Write Multiple command.
When the Write Multiple command is issued, the Sector Count Register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:
n = (sector count) module (block count).
If the Write Multiple command is attempted before the Set Multiple Mode command has been executed or when Write Multiple commands are disabled, the Write Multiple operation will be rejected with an aborted command error.
Errors encountered during Write Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.
The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count Register contains the residual number of sectors that need to be transferred for successful completion of the command. For example, each block has 4 sectors, a request for 8 sectors is

issued and an error occurs on the third sector. The Sector Count Register contains 6 and the address is that of the third sector.
Note: The current revision of the CompactFlash Memory Card only supports a block count of 1 as indicated in the Identify Drive Command information. The Write Multiple command is provided for compatibility with future products which may support a larger block count.
Table 83 defines the Write Multiple command Byte sequence.

Table 83: Write Multiple

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.27 Write Multiple without Erase (CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before write operation is not performed. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. Table 84 defines the Write Multiple without Erase command Byte sequence.

Table 84: Write Multiple without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	CDh							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.28 Write Sector(s) (30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the Card sets BSY, sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.
For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector. Table 85 defines the Write Sector(s) command Byte sequence.

Table 85: Write Sector(s)

Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h or 31h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.29 Write Sector(s) without Erase (38h)

This command is similar to the Write Sector(s) command with the exception that an implied erase before write operation is not performed. This command has the same protocol as the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector(s) command before this command is issued. If the sector is not pre-erased a normal write sector operation will occur. Table 86 defines the Write Sector(s) without Erase command Byte sequence.

Table 86: Write Sector(s) without Erase

Task File Register	7	6	5	4	3	2	1	0
COMMAND	38h							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

10.30 Write Verify (3Ch)

This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write Sector(s) command. Table 87 defines the Write Verify command Byte sequence.

Table 87: Write Verify

Task File Register	7	6	5	4	3	2	1	0
COMMAND	3Ch							
DRIVE/HEAD	1	LBA	1	D	Head (LBA 27-24)			
CYLINDER HI	Cylinder High (LBA23-16)							
CYLINDER LOW	Cylinder Low (LBA15-8)							
SECTOR NUM	Sector number (LBA7-0)							
SECTOR COUNT	Sector Count							
FEATURES	nu							

11 CIS information (typical)

```
0000: Code 01, link 04
DF 12 01 FF
```

- Tuple CISTPL_DEVICE (01), length 4 (04)
- Device type is FUNCSPEC
- Extended speed byte used
- Device speed is 120ns
- Write protect switch is not in control
- Device size is 2K bytes

```
000C: Code 1C, link 05
02 DF 12 01 FF
```

- Tuple CISTPL_DEVICE_0C (1C), length 5 (05)
- Device conditions : VCC = 3.3V
- Device type is FUNCSPEC
- Extended speed byte used
- Device speed is 120ns
- Write protect switch is not in control
- Device size is 2K bytes

```
001A: Code 18, link 02
DF 01
```

- Tuple CISTPL_JEDEC_C (18), length 2 (02)
- Device 0 JEDEC id: Manufacturer DF, ID 01

```
0022: Code 20, link 04
0A 00 00 00
```

- Tuple CISTPL_MANFID (20), length 4 (04)
- Manufacturer # 0x000A hardware rev 0.00

```
002E: Code 15, link 1B
04 01 53 57 49 53 53 42 49 54 00 xx xx xx 4D 42
20 43 46 20 43 41 52 44 00 00 FF
```

- Tuple CISTPL_VERS_1 (15), length 23 (17)
- Major version 4, minor version 1
- Product Information: Manufacturer: "SWISSBIT",
- Product name: "SFCFxxxxxxxxxx x xxx xxx" (part number)
- **The length of the strings will affect the following start addresses**

```
0068: Code 21, link 02
04 01
```

- Tuple CISTPL_FUNCID (21), length 2 (02)
- Function code 04 (Fixed Disk), system init 01

```
0070: Code 22, link 02
01 01
```

- Tuple CISTPL_FUNCE (22), length 2 (02)
- This is a PC Card ATA Disk

```
0078: Code 22, link 03
02 0C 0F
```

- Tuple CISTPL_FUNCE (22), length 3 (03)
- Vpp is not required
- This is a silicon device
- Identify Drive Model/Serial Number is guaranteed unique
- Low-Power Modes supported: Sleep Standby Idle
- Drive automatically minimizes power
- All modes include 3F7 or 377
- Index bit is not supported
- -IOIS16 is unspecified in Twin configurations

```
0082: Code 1A, link 05
01 03 00 02 0F
```

- Tuple CISTPL_CONFIG (1A), length 5 (05)
- Last valid configuration index is 3
- Configuration Register Base Address is 200
- Configuration Registers Present: Configuration Option Register at 200
- Card Configuration and Status Register at 202
- Pin Replacement Register at 204
- Socket and Copy Register at 206

```
0090: Code 1B, link 08
C0 C0 A1 01 55 08 00 20
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 8 (08)
- Configuration Table Index is 00 (default)
- Interface type is Memory
- BVDs not active, WP not active, RdyBsy active
- Wait signal support required
- VCC Power Description: Nom V = 5.0 V
- Map 2048 bytes of memory to Card address 0
- Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown

```
00A4: Code 1B, link 06
00 01 21 B5 1E 4D
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06)
- Configuration Table Index is 00
- VCC Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

```
00B4: Code 1B, link 0A
C1 41 99 01 55 64 F0 FF FF 20
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 10 (0A)
- Configuration Table Index is 01 (default)
- Interface type is I/O
- BVDs not active, WP not active, RdyBsy active
- Wait signal support not required
- VCC Power Description: Nom V = 5.0 V
- Decode 4 I/O lines, bus size 8 or 16
- IRQ may be shared; pulse and level mode interrupts are supported
- Interrupts in mask FFFF are supported
- Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown

```
00CC: Code 1B, link 06
01 01 21 B5 1E 4D
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06)
- Configuration Table Index is 01
- VCC Power Description: Nom V = 3.30 V,
- Peak I = 45.0 mA

```
00DC: Code 1B, link 0F
C2 41 99 01 55 EA 61 F0 01 07 F6 03 01 EE 20
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F)
- Configuration Table Index is 02 (default)
- Interface type is I/O
- BVDs not active, WP not active, RdyBsy active
- Wait signal support not required
- VCC Power Description:
- Nom V = 5.0 V
- Decode 10 I/O lines, bus size 8 or 16
- I/O block at 01F0, length 8
- I/O block at 03F6, length 2
- IRQ may be shared; pulse and level mode interrupts are supported
- Only IRQ14 is supported
- Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown

```
00FE: Code 1B, link 06
02 01 21 B5 1E 4D
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06)
- Configuration Table Index is 02
- VCC Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

```
010E: Code 1B, link 0F
C3 41 99 01 55 EA 61 70 01 07 76 03 01 EE 20
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 15 (0F)
- Configuration Table Index is 03 (default)
- Interface type is I/O
- BVDs not active, WP not active, RdyBsy active
- Wait signal support not required
- VCC Power Description: Nom V = 5.0 V
- Decode 10 I/O lines, bus size 8 or 16
- I/O block at 0170, length 8
- I/O block at 0376, length 2
- IRQ may be shared; pulse and level mode interrupts are supported
- Only IRQ14 is supported
- Miscellaneous Features: Max Twins 0, -Audio, -ReadOnly, +PowerDown

```
0130: Code 1B, link 06
03 01 21 B5 1E 4D
```

- Tuple CISTPL_CFTABLE_ENTRY (1B), length 6 (06)
- Configuration Table Index is 03
- VCC Power Description: Nom V = 3.30 V, Peak I = 45.0 mA

```
0140: Code 14, link 00
```

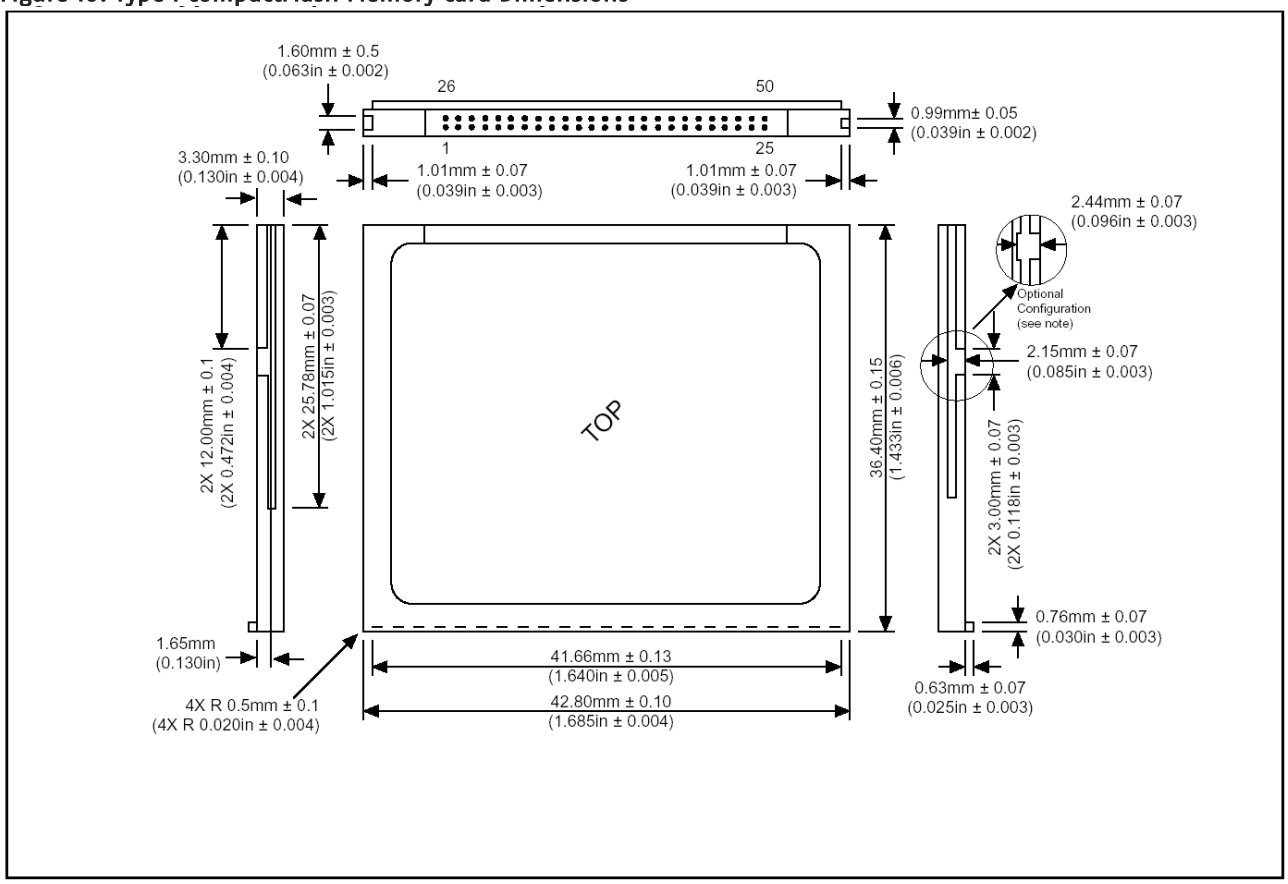
- Tuple CISTPL_NO_LINK (14), length 0 (00)

```
0144: Code FF
```

- Tuple CISTPL_END (FF)

12 Package mechanical

Figure 10: Type I CompactFlash Memory Card Dimensions



13 Declaration of Conformity

Product Type:	CompactFlash™ Card
Brand Name:	SWISSMEMORY™ CompactFlash™
Model Designation:	SFCFxxxxHxxxxxx-x-xx-xxx-xxx
Manufacturer:	Swissbit AG Industriestrasse 4-8 CH-9552 Bronschhofen Switzerland

The product complies with the requirements of the following directives:

CENELEC EN 55022B :2000 + CISPR22B :2000
CENELEC EN 55024 :2001 + CISPR24 :2001
FCC47 Part 15 Subpart B

The product was tested according all EMC requirements necessary for CE-mark

Year of the first marking: 2006

Silvio Muschter
Vice President
Engineering & Development

Bronschhofen, Oct 26, 2006

14 RoHS and WEEE update from Swissbit

Dear Valued Customer,

We at Swissbit place great value on the environment and thus pay close attention to the diverse aspects of manufacturing environmentally and health friendly products. The European Parliament and the Council of the European Union have published two Directives defining a European standard for environmental protection. This states that CompactFlash Cards must comply with both Directives in order for them to be sold on the European market:

- **RoHS** – Restriction of Hazardous Substances
- WEEE – Waste Electrical and Electronic Equipment

Swissbit would like to take this opportunity to inform our customers about the measures we have implemented to adapt all our products to the European norms.

What is the WEEE Directive (2002/96/EC)?

The Directive covers the following points:

- Prevention of WEEE
- Recovery, recycling and other measures leading to a minimization of wastage of electronic and electrical equipment
- Improvement in the quality of environmental performance of all operators involved in the EEE life cycle, as well as measures to incorporate those involved at the EEE waste disposal points

What are the key elements?

The WEEE Directive covers the following responsibilities on the part of producers:

Producers must draft a disposal or recovery scheme to dispose of EEE correctly.
Producers must be registered as producers in the country in which they distribute the goods.
They must also supply and publish information about the EEE categories.
Producers are obliged to finance the collection, treatment and disposal of WEEE.

Inclusion of WEEE logos on devices

In reference to the Directive, the WEEE logo must be printed directly on all devices that have sufficient space. «In exceptional cases where this is necessary because of the size of the product, the symbol of the WEEE Directive shall be printed on the packaging, on the instructions of use and on the warranty» (WEEE Directive 2002/96/EC)

When does the WEEE Directive take effect?

The Directive came into effect internationally on 13 August, 2005.

What is RoHS (2002/95/EC)?

The goals of the Directive are to:

- Place less of a burden on human health and to protect the environment by restricting the use of hazardous substances in new electrical and electronic devices
- To support the WEEE Directive (see above)

RoHS enforces the restriction of the following 6 hazardous substances in electronic and electrical devices:

- Lead (Pb) – no more than 0.1% by weight in homogeneous materials
- Mercury (Hg) – no more than 0.1% by weight in homogeneous materials
- Cadmium (Cd) – no more than 0.01% by weight in homogeneous materials
- Chromium (Cr6+) – no more than 0.1% by weight in homogeneous materials
- PBB, PBDE – no more than 0.1% by weight in homogeneous materials

Swissbit is obliged to minimize the hazardous substances in the products.

According to part of the Directive, manufacturers are obliged to make a self-declaration for all devices with RoHS. Swissbit carried out intensive tests to comply with the self-declaration. We have also already taken steps to have the analyses of the individual components guaranteed by third-party companies.

Swissbit carried out the following steps during the year with the goal of offering our customers products that are fully compliant with the RoHS Directive.

- **Preparing all far-reaching directives, logistical enhancements and alternatives regarding the full understanding and introduction of the RoHS Directive's standards**
- **Checking the components and raw materials:**
  - Replacing non-RoHS-compliant components and raw materials in the supply chain
  - Cooperating closely with suppliers regarding the certification of all components and raw materials used by Swissbit
- **Modifying the manufacturing processes and procedures**
  - Successfully adapting and optimizing the new management-free integration process in the supply chain
  - Updating existing production procedures and introducing the new procedures to support the integration process and the sorting of materials
- **Carrying out the quality process**
  - Performing detailed function and safety tests to ensure the continuous high quality of the Swissbit product line

When does the RoHS Directive take effect?

As of 1 July, 2006, only new electrical and electronic devices with approved quantities of RoHS will be put on the market.

When will Swissbit be offering RoHS-approved products?

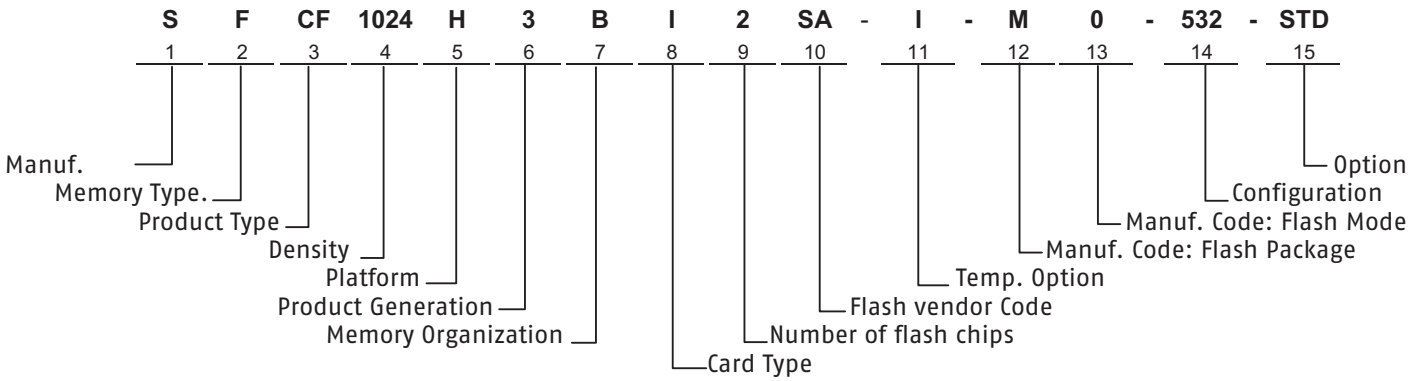
Swissbit's RoHS-approved products are available now. Please contact your Swissbit contact person to find out more about exchanging your existing products for RoHS-compliant devices.

For your attention

We understand that packaging and accessories are not EEE material and are therefore not subject to the WEEE or RoHS Directives.

Contact details:
Swissbit AG
Industriestrasse 4-8
CH 9552 Bronschhofen
Tel: +41 71 913 72 72 – Fax: +41 71 913 74 50
E-mail: info@swissbit.com – Website: www.swissbit.com

15 Part Number Decoder



15.1 Manufacturer

Swissbit code	S

15.2 Memory Type

Flash	F

15.3 Product Type

Compact Flash	CF

15.4 Density

128 MB	0128
256 MB	0256
512 MB	0512
1 GB	1024
2 GB	2048
4 GB	4096
8 GB	8192
16 Gbyte	16GB
32 Gbyte	32GB

15.5 Platform

Compact Flash	H

15.6 Productgeneration

15.7 Memory Organization

x8	B
x16	C

15.8 Card type

C-100	CF Card	I

15.9 Number of Flash Chip

1 Flash	1
2 Flash	2
4 Flash	4

15.10 Flash Code

Samsung	SA
Micron	MT
ST Microelectronics	ST
Hynix	HY
Intel	IT
Toshiba	TO
Infineon	IN

15.11 Temp. Option

Industrial Temp. Range -40°C – 85°C	I
Extended Temp. Range -25°C – 85°C	E
Standard Temp Range 0°C – 70°C	C

15.12 DIE Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q
MLC MONO (single die package)	G
MLC DDP (dual die package)	L
MLC QDP (quad die package)	H

15.13 PIN Mode

Normal nCE & R/nB	0
Dual nCE & Dual R/nB	1

15.14 Compact Flash XYZ

X→ CFC Mode

Removable/fix		PIO	DMA support	X
IDE-Mode	PC-Card			
Removable		yes	yes	1
Fix		yes	yes	2
Fix		yes	-	3
Removable		yes	-	4
Fix	Removable	yes	yes	5
Fix	Removable	yes	-	6

Y → Firmware Revision

FW Revision	Y
FW F0911	1
BB read out FW	2
FW G0622	3
Write Protect FW	4
Word49_bit11 FW	5

Z → max PIO-Mode / CIS

Max PIO Mode / CIS	Z
PIO4 standard CIS tuples	1
PIO6* standard CIS tuples	2

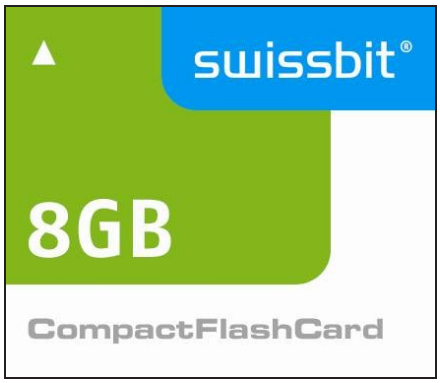
* The CF Advanced Timing Modes are not available if DMA operation is disabled on customer request.

15.15 Option

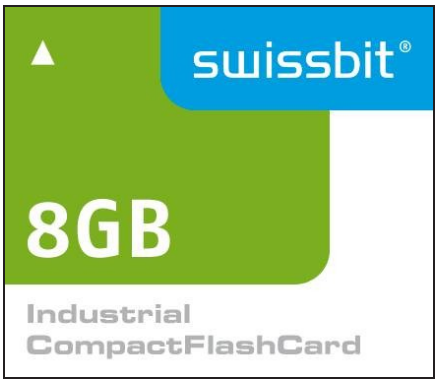
Swissbit / Standard	STD

16 Swissbit CF Label specification

16.1 Front side label

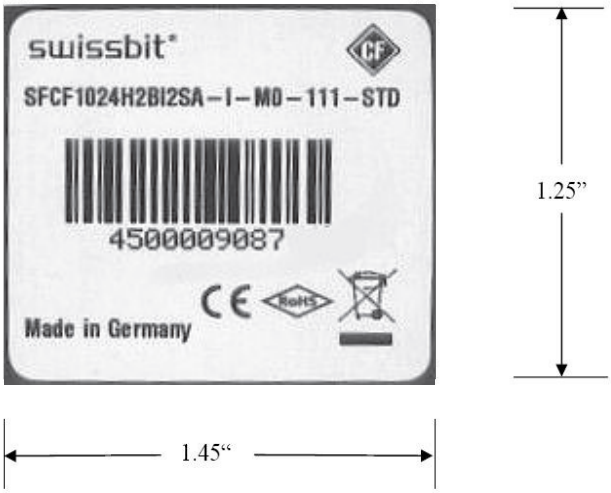


Commercial and extended CFC



Industrial CFC

16.2 Back side label



- Swissbit logo
- CF logo
- Part number (defined by the data sheet)
- Barcode as assembly lot number (Code128)
- CE logo
- RoHs logo
- WEEE logo
- Made in Germany string

17 Revision History

Table 88: Document Revision History

Date	Version		Revision Details
25-May-2007	1.00	First official release	Offered Options, min. 128MB
31-May-2007	1.01	Update, wear levelling	Corrected capacity 4GB, PCMCIA→ATA
21-June-2007	1.02	New options	Fix/removable options 5, 6 PIO6 option in CIS, host requirements for PIO6 (CF Spec 3.0)
29-June-2007	1.03	Update	Label and barcode spec
16-July-2007	1.04	Update	Drive geometry update
31-August-2007	1.05	Extended temp. range	New Market requirement: extended product category
12-October-2007	1.06	Add 64MB CFC; add FW adjustments	Update the performance value and new FW
25-January-2008	1.07	Update	Table 1-System Performance Update / Additional FW/16GB CHS Update
18-March-2008	1.08	Update	Back label information, PC card/IDE mode differences, switch delay; data retention
28-July-2008	1.10	Update	Add Serie reference
29-October-2008	1.20	new standard configuration	new standard part numbers (suffix -532), 16GB parameters, document structure
26-February-2009	1.21	Update	Correct PIO Mode by non DMA support; EOL 16GB