swissbit®

Product Data Sheet

Industrial SD Memory Card

S-250 Series
SPI and SD Compliant

Extended and Industrial Temperature Grade

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Made in Germany

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S-250 Series – Industrial SD Memory Card
512 MBytes up to 2 GBytes

1. Product Summary

- **Capacities:** 512 MBytes, 1 GBytes, 2 GBytes
- **Form Factor:** Standard SD Memory card form factor - 32.0mm x 24.0mm x 2.1mm, Write Protect slider
- **Compliance[1]:** Fully compliant with SD Memory Card specification 2.0 and Micro SD Memory Card specification 2.0 addendum
- **Environmental:** RoHS / REACH Compliant
- **Compatibility:** Supports SD SPI mode
- **Performance (max. capacity):**
  - SD burst up to 25MB/s
  - SD Low speed 0...25MHz clock rate
  - SD High speed 25...50MHz clock rate
  - Up to 24.2/13.5 MB/s sustained read/write speed
  - Flash burst up to 25MB/s
  - "Default speed cards" with disabled high speed mode available
- **Operating Temperature Range:**
  - Extended Temperature Range: -25° up to 85°C
  - Industrial Temperature range: -40° up to 85°C
- **Operating Voltage:** 2.7...3.6V normal operating voltage
- **Data Retention:** 10 years @ life begin; 1 year @ life end
- **High reliability:**
  - Best available SLC NAND Flash technology
  - Designed for embedded market
  - MTBF: > 3,000,000 hours
  - Number of insertions: > 10,000

[1] The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.

2. Product Features

- Wear Leveling: equal wear leveling of static and dynamic data.
  Wear leveling assures that dynamic data as well as static data is balanced evenly across the memory to guarantee the maximum write endurance of the device.
- Patented power-off reliability
  - No data loss of older sectors
  - Max. 16 sectors data loss (old data kept) if power off during writing
- Hot swappable
- Low-power CMOS technology
- Controlled "Locked" BOM
- Life Time Monitoring SD/SPI with standard or vendor commands

3. Ordering Information

Table 1: Standard Product List

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
512 MBytes	SFSD0512LgBN1WI-E-ME-1y1-STD	SFSD0512LgBN1WI-I-ME-1y1-STD
1 GByte	SFSD1024LgBN1WI-E-DE-1y1-STD	SFSD1024LgBN1WI-I-DE-1y1-STD
2 GBytes	SFSD2048LgBN1WI-E-QF-1y1-STD	SFSD2048LgBN1WI-I-QF-1y1-STD

g = product generation and y = firmware revision

Table 2: Available Part Numbers

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
512 MBytes	SFSD0512L1BN1WI-E-ME-111-STD	SFSD0512L1BN1WI-I-ME-111-STD
1 GBytes	SFSD1024L1BN1WI-E-DE-111-STD	SFSD1024L1BN1WI-I-DE-111-STD
2 GBytes	SFSD2048L1BN1WI-E-QF-111-STD	SFSD2048L1BN1WI-I-QF-111-STD

3.1 Offered options for customer projects

- Customer specified strings and IDs (MID, OID, PNM, PRV)
- Customer specified capacities
- Preload service
- Customized label and laser marking
- Permanent write protected (ROM) with preloaded software
- Default speed mode
- Diagnostic documentation for Card Status Register access or vendor command extension values

4. Product Description

The SD Memory Card is a small form factor non-volatile memory card which provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.

The Card operates in two basic modes:

- SD card mode
- SPI mode

The SD Memory Card also supports SD **High Speed mode** with up to 50MHz clock frequency.

The cards are compliant with

- SD Memory Card Specification Part 1, Physical layer Specification V2.00
- SD Memory Card Specification Part 2, File System Specification V2.00
- MICRO SD Memory Card Specification V1.10

Simplified specifications are available at https://www.sdcard.org/downloads/pls/index.html

The Card has an internal **intelligent controller** which manages interface protocols, data storage and retrieval as well as hardware RS-code **Error Correction Code (ECC), defect handling, diagnostics and clock control**.

The **wear leveling** mechanism assures an equal usage of the Flash memory cells to extend the life time.

The hardware RS-code ECC allows to detect and correct **4 symbols per 528 Bytes**.

The Card has a **voltage detector** and a powerful **power-loss management feature** to prevent data corruption after power-down. The power consumption is very low.

The cards are offered in 2 temperature ranges

- Extended -25°C...85°C
- Industrial -40...85°C

The cards are RoHS compliant and lead-free.

4.1 Performance Specifications

The S-250 read/write sequential performance benchmarks are detailed in Table 3.

Table 3: Read/Write Performance typical[2, 3]

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4k (IOPS)	Random Write 4k (IOPS)
512 MBytes	24.2	13.5	1580	29
1 GBytes				
2 GBytes				

4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in Table 4.

Table 4: Current Consumption

Current Consumption[4]	Typ	max	Unit
Write	50	70	mA
Read	42	60	
Sleep Mode	0.4	0.6	

[2] All values refer to Winbond Flash 4Gb 46nm
[3] Sustained Speed measured with USB-SD Memory Card reader with Crystal Disk Mark test tool version 6, 5x 100MB (512MB) / 500MB (1/2GB).
[4] @25°C

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions are provided in Table 5.

Table 5: Recommended Operating Conditions

Parameter	Value
Extended Operating Temperature	-25 °C to 85 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V (2.7V–3.6V)

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in Table 6.

Table 6: Recommended Storage Conditions[5]

Parameter	Value
Storage Temperature	-40 °C to 85 °C

4.3.3 Environmental Conditions

The Environmental Conditions are listed in Table 7.

Table 7: Environmental Conditions

Parameter	Value
Non-Operating Shock	Typ. 50g acceleration IEC 512-4-6c
Non-Operating Vibration	50G, 1.5mm p-p, 20..2000Hz, Sweep xyz-axis, five pulses each, Non operating MIL-STD-883 M2007.3 Condition B
Humidity (Non-Condensing)	Operation: 95%@25°C Storage: 93%@40°C 500h
Bending	30N SDA Part1 App E.1.
Torque	0.15Nm ±2.5° max SDA Part1 App E.1.

4.4 Mechanical Specifications

Physical dimensions are detailed in Table 8.

Table 8: Physical Dimensions

Physical Dimensions		Unit
Length	32.0±0.1	mm
Width	24.0±0.1	
Thickness (Max)	2.1 ±0.15	
Weight (Max Capacity)	2	g

[5] The data retention time at temperature above 40°C is reduced. Swissbit can provide more data and support on request.

4.5 Reliability

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in Table 9. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 9: Reliability[6]

Parameter	Value[7]
MTBF (at 25 °C)	> 3,000,000 hours
Data Retention	10 Years at Start (JESD47), 1 Year at EOL

4.6 Endurance

Endurance represented as TeraBytes Written (TBW) is provided in the following Table 10:

Table 10: Endurance[8, 9]

Drive Capacity	TeraBytes Written (TBW) @ Seq. Write 1MB Operation	TeraBytes Written (TBW) @ Random Write 128kB Operation	TeraBytes Written (TBW) @ Random Write 4kB Operation
512 MBytes	50	25	0.8
1 GBytes	102	51	1.6
2 GBytes	206	102	3.2

4.7 Drive Geometry Specification

The S-250 drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown in Table 11.

Table 11: Drive Geometry

Raw Capacity	User Capacity[10]	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
512 MBytes	512 MBytes	998,912	511,442,944
1024 Mbytes	1 GByte	2,001,920	1,024,983,040
2048 Mbytes	2 GBytes	4,016,128	2,056,257,536

[6] NAND Flash data retention and endurance characteristics are defined according to JEDEC JESD47 and JESD22. The endurance limits of the storage shall be monitored by the life time information and simulated before field usage by the customer.

[7] After every power on the card reads the whole flash and performs a data refresh if necessary. Therefore, the data retention can be much longer in most use cases.

[8] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

[9] Sequential write 1MB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

[10] 1 GByte = 10^9 bytes

5. Electrical Interface

The pad locations of the SD Memory Card are shown in Figure 1. The pad assignments and descriptions are listed in Table 11.

Figure 1: SD Memory Card Shape and Interface (Bottom View)

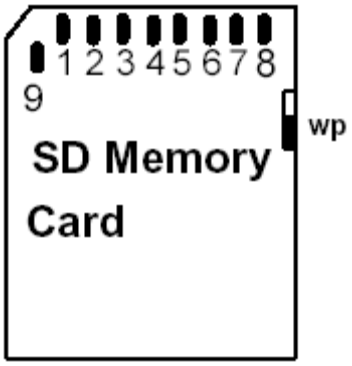


Table 12: SD Memory Card Pad Assignment SD Mode

Pin	SD Mode		
	Name	Type[11]	Description
1	CD/DAT3[12]	I/O/PP[13]	Card Detect/Data Line [Bit 3]
2	CMD	PP	Command/Response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1[14]	I/O/PP	Data Line [Bit 1]
9	DAT2[15]	I/O/PP	Data Line [Bit 2]

Table 13: SD Memory Card Pad Assignment SPI Mode

Pin	SPI Mode		
	Name	Type[11]	Description
1	CS	I[13]	Chip Select (neg true)
2	DI	I	Data In
3	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		
9	RSV		

[11] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
[12] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
[13] At power up this line has a 50kOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
[14] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
[15] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

5.1 DC characteristics

Measurements are at Recommended Operating Conditions unless otherwise specified.

Table 14: DC Characteristics

Symbol	Parameter	min(1)	typ(1)	max(1)	unit	notes
I_{DD}	Operating Current Read		40	60	mA	@ 25°C
	Operating Current Write		50	70	mA	@ 25°C
	Pre-initialization Standby Current		150	200	µA	@ 25°C
	Post-initialization Standby Current		130	150	µA	@ 25°C
			400	600	µA	@ 85°C
I_{LI}	Input Leakage Current	-10		10	µA	without pull up R
I_{LO}	Output Leakage Current	-10		10	µA	

1) Target values

Table 15: SD Memory Card Recommended Operating Conditions

Symbol	Parameter		min	typ	max	unit
V_{DD}	Supply Voltage	Normal Operating Status	2.7	3.3	3.6	V
		Basic Communication (CMD0, CMD15, CMD55, ACMD41)	2.0	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

5.2 Signal Loading

according to SD specification

5.3 AC characteristics

5.3.1 Default Speed mode (0 – 25MHz)

according to SD specification

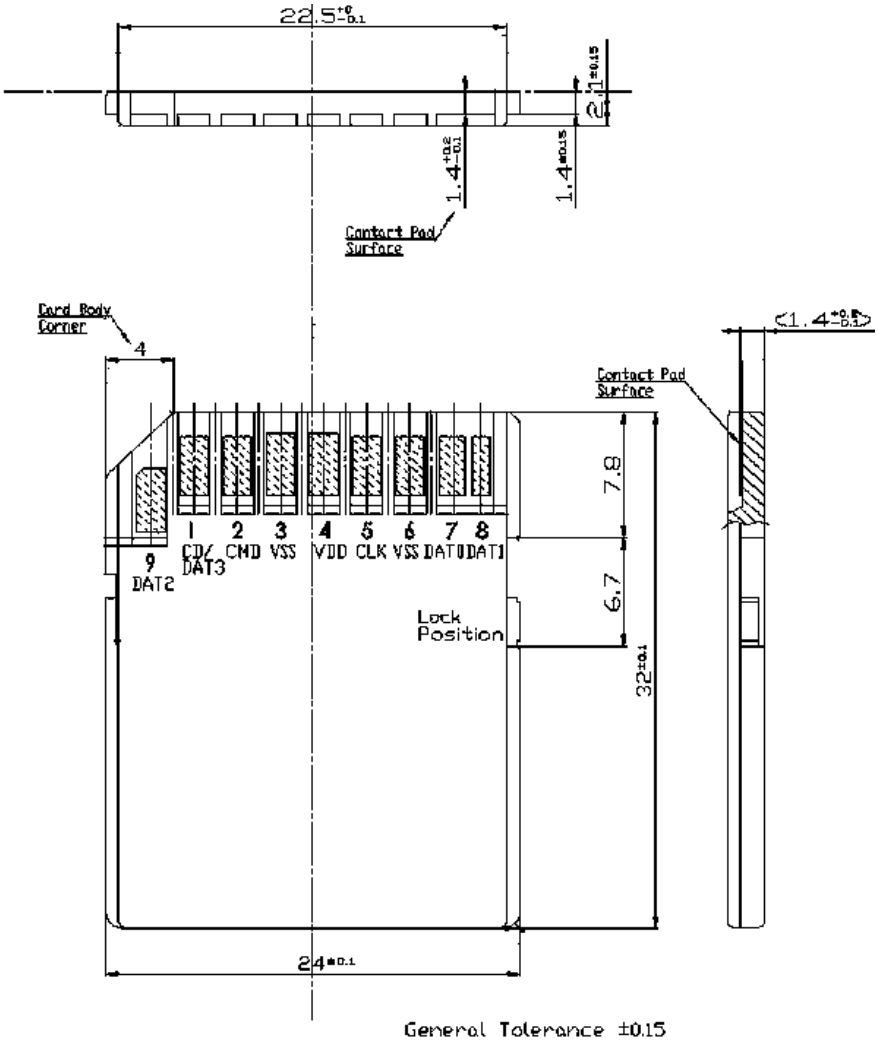
5.3.2 High Speed mode (0 – 50MHz)

according to SD specification

6. Package Mechanical

The SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).
The dimensions and tolerances are according to the SD specification.

Figure 2: Simplified mechanical dimensions SD card



The dimensions and tolerances are according to the SD specification.

7. Host access Specification

The following chapters summarize how the host accesses the card:

- Chapter 7.1 summarizes the SD and SPI buses.
- Chapter 7.2 summarizes the registers.

7.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

7.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

7.1.2 SPI Bus Mode Protocol

The Serial Peripheral Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal. The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional *dataIn* and *dataOut* signals.

Table 16: SPI Bus Signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

7.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in *idle_state*. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.
The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available.
During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should re-start the card as Multimedia Card using CMD0 and CMD1.

7.2 Card Registers

The SD Memory Card has five registers. Refer to Table 17 to Table 22 for detail.

Table 17: SD Memory Card registers

Register Name	Bit Width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA	16	Relative Card Address	This register carries the card address is SD Memory Card mode.

Table 18: CID register

Register Name	Bit Width	Description	typ. value
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	"LgBNc" g=generation c=number of channels
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

Table 19: OCR register

OCR bit position	VDD voltage window	typ. value	OCR bit position	VDD voltage window	typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24-30	Reserved	
13	2.5-2.6	0	30	Card Capacity Status (CCS)	*(1)
14	2.6-2.7	0	31	0=busy; 1=ready	*(2)

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.

Table 20: CSD register

Register Name	First Bit	Bit Width	Description	typ. Value
CSD_STRUCTURE	127	2	CSD structure	00
–	125	6	Reserved	000000
TAAC	119	8	Data read access time 1	00001110
NSAC	111	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103	8	Data transfer rate	00110010
CCC	95	12	Card command classes	010110110101
READ_BL_LEN	83	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	1
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75	2	Reserved	00
C_SIZE	73	12	Device size	xxx(1)
VDD_R_CURR_MIN	61	3	VDD min read current	110
VDD_R_CURR_MAX	58	3	VDD max read current	110
VDD_W_CURR_MIN	55	3	VDD min write current	110
VDD_W_CURR_MAX	52	3	VDD max write current	110
C_SIZE_MULT	49	3	Device size multiplier	110(1)
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45	7	Erase sector size	1111111
WP_GRP_SIZE	38	7	Write protect group size	0000011(1)
WP_GRP_ENABLE	31	1	Write protect group enable	0

Register Name	First Bit	Bit Width	Description	typ. Value
–	30	2	Reserved	00
R2W_FACTOR	28	3	Write speed factor	100
WRITE_BL_LEN	25	4	Write data block length	1010(1)
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(*)
COPY	14	1	Copy flag	0 W(*)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(*)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11	2	File format	00 W(*)
–	9	2	Reserved	00 W
CRC	7	7	Checksum of CSD contents	xxxxxxx W
–	0	1	Always=1	1

1) Drive Size and block sizes may vary with card capacity and firmware generation
memory capacity = BLOCKNR * BLOCK_LEN
Where
BLOCKNR = (C_SIZE+1) * MULT
MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
BLOCK_LEN = $2^{READ\_BL\_LEN}$, (READ_BL_LEN < 12)

W value can be changed with CMD27 (PROGRAM_CSD)
W(*) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 21: SCR register

Field	Bit Width	typ Value
SCR_STRUCTURE	4	0000
SD_SPEC	4	0010
DATA_STAT_AFTER_ERASE	1	1
SD_SECURITY	3	011
SD_BUS_WIDTHS	4	0101
Reserved	16	0
Reserved	32	0

Table 22: RCA register

Field	Bit Width	typ Value
RCA	16	0x0000(1)

1) After Initialization the card can change the RCA register.

8. Card Lifetime Information Data

Swissbit S-250 cards provide various lifetime monitoring information in the "reserved for manufacturer" field of the SD Status register. This data can be read out using ACMD13 (SD_STATUS) on host systems with a native SD-Interface (e.g. embedded systems, SD or SPI interface or PCI/SD-reader).
We recommend assessing the expected/guaranteed life time of Flash based devices to make sure the product life time fulfills your expectations. The real application workload should be tested in a test installation or simulation for best accuracy.
In general, calculations based on application behavior statistics are not possible as the influence of the operating systems (with the caches) and the file system have a big influence on the data actually written on the device.
This product does report the real erase cycles that the NAND Flash blocks have seen. Based on the average erase count and it's ascend in the target system, it is possible to quite simply calculate the expected life time of the product.
Bad and spare block counts can't be used for linear life time calculations. In the beginning of the device life time, only very few blocks will be needed to be replaced. Generally if a device reaches the end of the lifetime, more bad blocks will occur.
The SD Status is defined by the SD Standard and contains several status bits as well as a field for manufacturer specific data. The overall size of the SD Status is one data block of 512 bits divided into 312 reserved for manufacturer bits used for the Swissbit lifetime information and 200 bits for other purposes, defined by the SDA.
The content of the SD Status register is transmitted to the Host over the DAT bus along with a 16-bit CRC. The SD Status is sent to the host over the DAT bus as a response to ACMD13 (CMD55 followed with CMD13). ACMD13 can be sent to a card only in "tran_state" (card is selected).

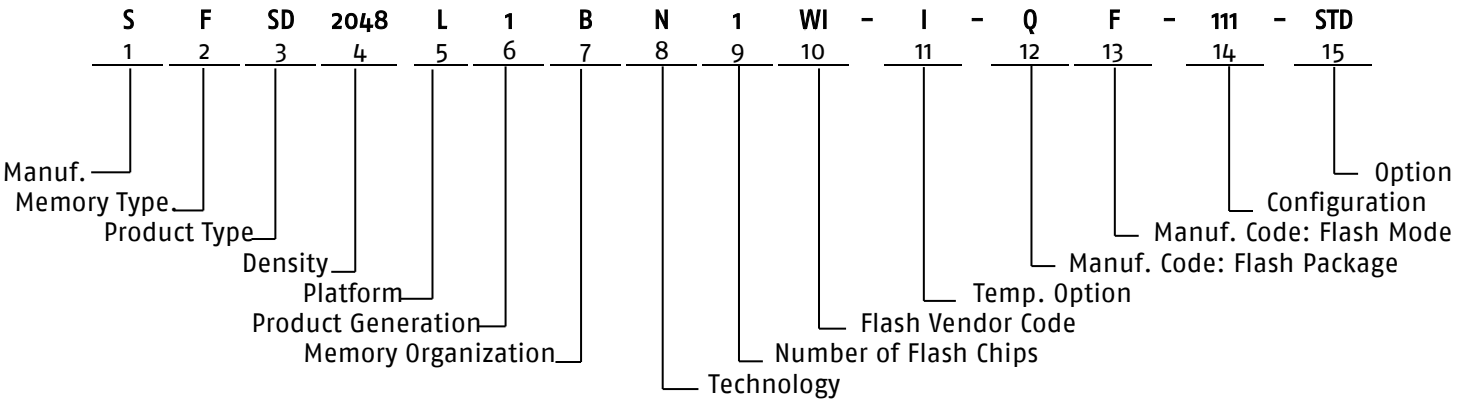
Please note that it is not possible so set up the necessary command (ACMD13) through a common USB/SD-card reader/bridge. In contrast to that, a lot of embedded systems and PCIe card readers support the command. Swissbit provides a demo code written in C for Linux systems on demand.

Table 23: SD Status and Lifetime Information sector decoding

Bits	Description (All values MSb first)
[511:312]	SD Status field as defined in the Physical Layer Specification Version 2.00 (Not relevant for Card Lifetime Info)
[311:304]	Data structure version identifier ("0" for S-200/S-220 cards)
[303:288]	Number of initial defect blocks
[287:272]	Number of initial spare blocks, 1st flash CE (across channels) big Endian
[271:256]	Number of initial spare blocks, 2nd flash CE (across channels) big Endian
[255:248]	Percentage of remaining spare blocks, first flash CE (across channels)
[247:240]	Percentage of remaining spare blocks, second flash CE (across channels)
[239:224]	(Reserved)
[223:192]	(Reserved)
[191:176]	Lowest wear level class (WL)
[175:160]	Highest wear level class (WH)
[159:144]	Wear level threshold (T)
[143:96]	Total number of block erases
[95:80]	Number of flash blocks
[79:64]	Maximum flash block erase count target, in wear level class units
[63:32]	Power on count
[31:24]	(Reserved)
[23:16]	(Reserved)
[15:8]	(Reserved)
[7:0]	(Reserved)

The lowest wear level class (WL) and highest wear level class (WH) fields give the range of wear level classes currently in use. The wear level threshold (T) gives the size of a wear level class, minus 1, in units of flash memory block erases. Thus, the number of block erases that the flash blocks have seen is between WL*(T+1) and WH*(T+1)-1.

9. Part Number Decoder



9.1 Manufacturer

Swissbit code	S

9.2 Memory Type

Flash	F

9.3 Product Type

SD Memory Card	SD

9.4 Density

512 Mbytes	0512
1 GBytes	1024
2 GBytes	2048

9.5 Platform

SD Memory Card	L

9.6 Product Generation

9.7 Memory Organization

x8	A

9.8 Technology

S-250 Series	X

9.9 Number of Flash Chips

1 Flash Channel	1

9.10 Flash Code

Windbond	WI

9.11 Temperature Option

Industrial Temp. Range -40°C – 85°C	I
Extended Temp. Range -25°C – 85°C	E

9.12 Die Classification

SLC MONO (single die package)	M
SLC DDP (dual die package)	D
SLC QDP (quad die package)	Q

9.13 Pin Mode

Single nCE & R/nB	E
Dual nCE & Dual R/nB	F

9.14 Drive configuration XYZ

X = Configuration

Configuration	X
Default	1

Y = Firmware Revision

FW Revision	Y
Standard	1

Z = Optional

Optional	Z
Default	1
Default Speed	2
Default Speed, 12mA driver strength	3

9.15 Option

Standard	STD
Customer specific	XXX

10. Marking Specification

10.1 Top View

Figure 3: S-250 top view

10.2 Bottom view

Figure 4: S-250 bottom view

Swissbit
Part number

Manufacturing date / Lot code

Made in Germany

CE / WEEE logo

11. Revision History

Table 24: Document Revision History

Date	Revision	Description	Revision Details
07-Aug-2020	1.00	Initial release	Doc. req. no. 3965
21-Oct-2020	1.01	Updated random performance, added endurance	Doc. req. no. 4109
26-Nov-2020	1.02	Updated random performance and product illustration	Doc. req. no. 4221