Noritake itron

VACUUM FLUORESCENT DISPLAY

MODULE

SPECIFICATION

MODEL: CU20025ECPB-W1J

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This product complies with RoHS Directive 2002/95/EC

1. General Description

1.1 Application :

Readout of computer, micro-computer, communication terminal and automated instruments.

1.2 Construction :

Single board display module consists of 40 characters(2 x 20) VFD, one chip controller driver which has character generator ROM and RAM, DC/DC converter.

1.3 Scope

Interface level is TTL-8/4 bit parallel and the module can be connected to the CPU bus directly. +5V single power supply is required.

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
Power Supply Voltage	Vcc	0		5.5	VDC	
Logic Input Voltage	VI	0		Vcc	VDC	

3. Electrical Ratings

Conditions :Ta=25°C

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Logic Input Voltage	"H"	Vін	2.0		Vcc	VDC	$V_{CC} = E_{CV}$
	"L"	VIL	0		0.8	VDC	VCC - 5.0V
Power supply Voltag	je	Vcc	4.75	5.00	5.25	VDC	

4. Electrical Characteristics

Conditions : $Ta = 25^{\circ}C$, VCC=5.0V

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
Logic Output Voltage	"H"	Vон	VCC-0.4	—	—		ІОН = -1.60mA
	"L"	VOL		-	0.4	VDC	IOL = 1.60 mA
Power Supply Currer	ICC 1		130	200	mA	Display ON	
Power Supply Currer	ICC 2	—	2	10	mA	Display OFF	

Note : ICC1 shows the current, when all dots are turned on. Slow-start power supply may cause a failure of Power-on reset which is explained in " 8.2 Power-on reset". The power supply is recommended to be quick switch-on type(quicker than 50msec).

ICC1 might be anticipated twice as usual at power on rush.

5. Optical Characteristics

Number of characters	: 40 (2 lines x 20 chars)
Matrix format	: 5 x 7 dot with underline
Display area	: 70.8 x 11.5mm (X x Y)
Character size	: 2.4 x 4.7 mm (X x Y) Underline is not included.
Character pitch	: 3.6 mm
Line pitch	: 6.1 mm
Dot size	: 0.4 x 0.5mm (X x Y)
Dot pitch	: 0.5 x 0.7mm (X x Y)
Luminance Color of illumination	: 350 cd/m ² (100fL) Min. : Blue-Green

6. Environmental Conditions

Operating temperature : -40	to +85℃
Storage temperature : -50	to +85℃
Operating humidity : 20 t	0 80 % RH (Non condensation)
Vibration(Non operation): 10 t	o 55 to 10 Hz(Frequency),
1.0	mm(Total Amplitude)
30	Vin.(Duration)
Х, Ү	,Z each direction
Shock (Non operation): 539	m/S ² , 10mS

7. Functional Descriptions

7.1 Instruction table

Instruction	CODE										Cycle	Description	
Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Time	Description	
Display clear	0	0	0	0	0	0	0	0	0	1	2.3 ms Max.	Clears all display and sets DD RAM address 0 in the address counter.	
Cursor home	0	0	0	0	0	0	0	0	1	*	1*tCYC	Sets DD RAM address 0 in the address counter. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	1*tCYC	Sets the cursor direction and specifies display shift. These operations are performed during writing/reading data.	
Display ON/OFF control	0	0	0	0	0	0	1	D	с	В	1*tCYC	Sets all display ON/OFF(D),cursor ON/OFF(C),cursor blink of character position (B).	
Cursor or display shift	0	0	0	0	0	1	S/C	R/L	*	*	1∗tCYC (2∗tCYC)	Shifts display or cursor, keeping DD RAM contents.	
Function set	0	0	0	0	1	IF	*	*	*	*	1*tCYC	Sets data length (IF).	
Bright- ness control	1	0	*	*	*	*	*	*	BR1	BR0	1+tCYC	Accepts 1 byte data of just after "Function set" as brightness control data.	

CU20025ECPB-W1J

Instruction					T :	Description						
Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	rime	Description
CG RAM address setting	0	0	0	1	1 ACG					1*tCYC (2*tCYC)	Sets the CG RAM address.	
DD RAM address setting	0	0	1		ADD						1+tCYC (2+tCYC)	Sets the DD RAM address.
Busy flag & address reading	0	1	BF		ACC							Reads busy flag (BF) and address counter.
Data writing to CG or DD RAM	1	0			Data writing							Writes data into CG RAM or DD RAM.
Data read- ing from CG or DD RAM	1	1			Data reading						1 *tCYC	Reads data from CG RAM or DD RAM.
	I/D = 1: IncrementIF = 1:8-b $I/D = 0$: DecrementIF = 0:4-b $S = 1$: Display shift enabledBF = 1: Bu $S = 0$: Cursor shift enabledBF = 0: No $S/C = 1$: Display shiftbu $S/C = 0$: Cursor moveBF = 0: No $R/L = 1$: Shift to the rightBF $R/L = 0$: Shift to the leftBR1,BR0 =00: 100%01: 75%10: 50%11: 25%								hit Isy Isy		DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG: CG RAM address ADD: DD RAM address ACC: Address Counter	

Note:

*

: don't care

- tCYC : tCYC is read/write cycle (Min1us) of HOST SYSTEM.
- () : If RAM read is a next operation, needs execution time indicated by "()".

7.2 Display Clear

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0



This instruction

- 1. Fills all locations in the display data (DD) RAM with 20H(Blank character).
- 2. Clears the contents of the address counter to 0H.
- 3. Sets the display for zero character shift.
- 4. Sets the address counter to point to the DD RAM.
- 5. If the cursor is displayed, moves the cursor to the left most character in the top line (line 1).
- 6. Sets the address counter to increment on each access of DD RAM or CG RAM.
- 7.3 Cursor Home



This instruction

- 1. Clears the contents of the address counter to 0H.
- 2. Sets the address counter to point to the DD RAM.
- 3. Sets the display for zero character shift.
- 4. If the cursor is displayed, moves the left most character in the top line (line 1).

7.4 Entry Mode Set

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

0	0	0	0	0	1	I/D	S	04H to 07H
	RS=	0						

The I/D bit selects the way in which the contents of the address counter are modified after every access to DD RAM or CG RAM.

I/D=1: The address counter is incremented.

I/D=0: The address counter is decremented.

The S bit enables display shift, instead of cursor shift, after each write or read to the DD RAM.

S=1: Display shift enabled.

S=0: Cursor shift enabled.

The direction in which the display is shifted is opposite in sense to that of the cursor. For example if S=0 and I/D=1, the cursor would shift one character to the right after a CPU writes to DD RAM. However if S=1 and I/D=1, the display would

shift one character to the left and the cursor would maintain its position on the panel.

The cursor will already be shifted in the direction selected by I/D during reads of the DD RAM, irrespective of the value of S. Similarly reading and writing the CG RAM always shifts the cursor. Also both lines are shifted simultaneously.

I/D	S	After writing DD RAM data	After reading DD RAM data							
0	0	The cursor moves one character to the left.	The cursor moves one character to the left.							
1	0	The cursor moves one character to the right.	The cursor moves one character to the right.							
0	1	The display shifts one character to the right without cursor's move.	The cursor moves one character to the left.							
1	1	The display shifts one character to the left without cursor's move.	The cursor moves one character to the right.							

Cursor move and Display shift by the "Entry Mode Set"

7.5 Display ON/OFF

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

0	0	0	0	1	D	С	В	08H to 0FH
	RS=	0						

This instruction controls various features of the display.

The D bit turns the entire display on or off.

D=1: Display on

D=0: Display off

Note: When display is turned off, power converter also inhibited and reduce a power consumption.

The C bit turns the cursor on or off.

C=1: Cursor on

C=0: Cursor off

The B bit enables blinking of the character the cursor coincides with.

B=1: Blinking on

B=0: Blinking off

Blinking is achieved by alternating between a normal and all on display of a character. The cursor blinks with a frequency of about 1.1 Hz and DUTY 50%.

7.6 Cursor/Display Shift





This instruction shifts the display and/or moves the cursor, on character to the left or right, regardless of a DD RAM write/read.

The S/C bit selects movement of the cursor or movement of both the cursor and the display.

S/C=1: Shift both cursor and display.

S/C=0: Shift cursor only.

The R/L bit selects leftward or rightward movement of the display and/or cursor.

R/L=1: Shift one character right.

R/L=0: Shift one character left.

Cursor move and Display shift by the "Cursor/Display Shift"

S/C	R/L	Cursor shift	Display shift
0	0	Move one character to the left	No shift
0	1	Move one character to the right	No shift
1	0	Shift one character to left with display	Shift one character to the left
1	1	Shift one character to right with display	Shift one character to the right

7.7 Function Set

This command sets width of data bus line by itself, and sets screen brightness by following one byte data.

7.7.1 Function Set Command



This instruction initializes the system, and must be the first instruction executed after power-on. The IF bit selects between an 8-bit or a 4-bit bus width interface.

IF=1: 8-bit CPU interface using DB7 to DB0 IF=0: 4-bit CPU interface using DB7 to DB4

7.7.2 Brightness Control



One byte data (RS = 1) which follows the "Function Set Command" is considered as brightness data. When a command (RS=0) is written after the "Function Set Command ", the brightness control function is not initiated. Screen brightness is as follows;

BR1	BR0	Brightness
0	0	100 % (Default)
0	1	75 %
1	0	50 %
1	1	25 %

7.8 Set CG RAM Address

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

40H to 7FH

RS=0

I. Loads a new 6-bit address into the address counter.

2. Sets the address counter to address CG RAM.

Once "Set CG RAM Address" has been executed, the contents of the address counter will be automatically modified after every access of CG RAM, as determined by the "7.4 Entry Mode Set" instruction. The active width of the address counter, when it is addressing CG RAM, is 6-bit so the counter will wrap around to 00H from 3FH if more than 64 bytes of data are written to CG RAM.

7.9 Set DD RAM Address

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

 1
 ADD
 80H to A7H(1 line)

 RS=0
 C0H to E7H(2 line)

This instruction

1. Loads a new 7-bit address into the address counter.

2. Sets the address counter to point to the DD RAM.

Once the "Set DD RAM Address" instruction has been executed, the contents of the address counter will be automatically modified after each access of DD RAM, as selected by the "7.4 Entry Mode Set" instruction.

Valid DD RAM Address Ranges

	Number of Characters	ADR
1st line	40	00H to 27H
2nd line	40	40H to 67H

7.10 Write Data

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

DATA WRITE 00H to FFH

RS=1

This instruction writes the data in DB7 to DB0 into either the CG RAM or the DD RAM. The RAM space (CG or DD), and the address in that space, that is accessed depends on whether a "Set CG RAM Address" or a "Set DD RAM Address" instruction was last executed, and on the parameters of that instruction. The contents of the address counter will be automatically modified after each 'Write Data", as determined by the"7.4 Entry Mode Set". When data is written to the CG RAM, the DB7, DB6 and DB5 bits are not displayed as characters.

7.11 Read Data

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0

DATA READ

This instruction reads data from either CG RAM or DD RAM, depending on the type of "Set RAM Address" instructions last sent. The address in that space depends on the "Set RAM Address" instructions parameters. Immediately before executing "Read Data", "Set CG RAM Address" or "Set DD RAM Address" must be executed. The contents of the address counter are modified after each "Read Data". as determined by the "7.4 Entry Mode Set". Display shift is not executed, as described at the "7.4 Entry Mode Set".

7.12 Read Busy Flag/Address Counter

DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 BF ACC RS=0

Reading the instruction register yields the current value of the address counter and the

busy flag. This instruction must be executed prior to any other instructions. ACC, the address counter value, will point to a location in either CG RAM or DD RAM, depending on the type of "Set RAM Address" instruction last sent.

In "Busy Flag Check" immediately after executing "Write Data" instruction, a valid address counter value can be ready as soon as BF goes low. The BF bit shows the status of the busy flag.

BF = 1 : The display module is busy.

BF = 0: The display module is ready for next instruction.

8 Other features

8.1 CG RAM

The display module has CG RAM of 320 bit = $(5x8 \text{ bit /char}) \times 8$ chars which is for user definable character fonts. The character fonts consists of 5×7 dots with underline. The number 1 ~ 36 corresponds to character fonts.

Character code		CG	RAM	addı	ress		CG RAM data (character pattern))		
	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	0	0	0	0	0	*	*	*	1	2	3	4	5
	0	0	0	0	0	1	*	*	*	6	7	8	9	10
	0	0	0	0	1	0	*	*	*	11	12	13	14	15
00H	0	0	0	0	1	1	*	*	*	16	17	18	19	20
(08H)	0	0	0	1	0	0	*	*	*	21	22	23	24	25
	0	0	0	1	0	1	*	*	*	26	27	28	29	30
	0	0	0	1	1	0	*	*	*	31	32	33	34	35
	0	0	0	1	1	1	*	*	*	36	0	0	0	0
	0	0	1	0	0	0	*	*	*	1	2	3	4	5
	0	0	1	0	0	1	*	*	*	6	7	8	9	10
	0	0	1	0	1	0	*	*	*	11	12	13	14	15
01H	0	0	1	0	1	1	*	*	*	16	17	18	19	20
(09H)	0	0	1	1	0	0	*	*	*	21	22	23	24	25
	0	0	1	1	0	1	*	*	*	26	27	28	29	30
	0	0	1	1	1	0	*	*	*	31	32	33	34	35
	0	0	1	1	1	1	*	*	*	36	0	0	0	0

REMARKS ; "*" : Don't care

"0": Turned off

"1": Turned on.

Dot assignment

1	2	3	4	5				
6	7	8	9	10				
11	12	13	14	15				
16	17	18	19	20				
21	22	23	24	25				
26	27	28	29	30				
31	32	33	34	35				
	36							

___ Dot 36 is an under line.

8.2 Power-on reset

Internal status of the module is initialized, when the controller detects the rising of power supply. The status are as follows;

1. Display clear

Fills the DD RAM with 20Hex (Space code). During executing of "Display Clear" (Max 2.3msec), the busy flag(BF) is "1".

- 2. Clears the address counter to 0H. Sets the address counter to point the DD RAM.
- 3. Display ON/OFF

D=0:	Display OFF
C=0:	Cursor OFF
B=0:	Blink OFF

- 4. Entry Mode Set I/D =1: Increment(+1) S=0: No display shift
- 5. Function Set

IF=1: 8-bit interface

- 6. Brightness Control BR0=BR1=0 : 100%
- Remarks

There is a possibility that reset doesn't work by slow-start power supply . Therefore the initializing by commands is needed.

8.3 CPU interface

The display module is capable to communicate some different type of bus systems such as i80 or M68 ,8-bit or 4-bit data.

8.3.1 Select CPU

The module is able to connected to bus of i80 type or M68 type CPU, by setting JP2 jumper. Refer to "8.5 Jumper" for detail.

8.3.2 4-Bit CPU interface

If 4-bit interface is used, the 8-bit instruction are written nibble by nibble: the high-order nibble being written first, followed by low-order nibble. It is not necessary to check the busy flag between writing separate nibbles of individual instructions.

See "7.7.1 Function Set Command " for more information.

8.5 Jumper

Some jumper are prepared on the PCB board, to set operating mode of the display module. A soldering iron is required to short jumper.

No 2 and No 3 of the jumper 'JP1' is used to reset of module.

You can reset the module by shorting No 2 and No 3 of the jumper 'JP1' for some interval which is longer than 10 us.

The following figure shows the location of each jumper.

Location



The following table shows the function of No 1 and No 2 of JP1, JP2.

CU20025ECPB-W1J is no reset inputs from third hole of 14 through holes and M68 CPU bus interface. Reset input signal is active when it is low.

No1 and No 2 of JP1	third hole of 14 through holes
open	NC
short	RESET

NC:no connection

Table of JP2 setting

JP2	CPU bus mode	Control Signals
open	M68 type	E,R/W
short	i80 type	WR, RD

JP3 and JP4 is factory use only .

9 Character Font

ლი-ი	D 7 D 6 D 5 D 4		0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	
0000	0							•	÷						····.		
0001	1								-:::					.	÷;		
0010	2			::					ŀ			:		: <u>.</u>			
0011	3					: 	:;	:							.	:	::: :
0100	4			:	4				÷			•.		ŀ.	-	.	
0101	5											::					
0110	6					.	.	÷	:		·		<u>;</u>			<i>.</i>	
0111	7	- - - -		:	:				<u></u> .				-				
1000	8			÷					:::		:				Ņ		
1001	9		.					:	<u>اين</u>	<u>ن</u>	Ę	1	Ť	Ļ		•••	·!
1010	Α		:::: ::::	::	::											:	
1011	В		:: :::		:: ::	K.		H:			:	:*	Ţ			::	
1100	С		·#.	:						•••		* **				: : :-	
1101	D		ŀ											·			
1110	Ε		4	::			···.			::;:	· .				÷		
1111	F		.:	·					÷		·		<u>ا.</u> :				

Character Table 0 [CG57103]

Note: Font number 00~07Hex (08~0FHex) is UDF.

10. Timing



10.4 CPU bus read timing (M68 type)

- 11. Connector Pin assignment
- 11.1 14pin Connector

Fourteen (14) of through holes are prepared for power supply and data communications. A connector or pins may be able to soldered to the holes.

No.	Terminal	No.	Terminal
1	GND	8	DB1
2	Vcc	9	DB2
3	ЖNС	10	DB3
4	RS	11	DB4
5	R/W (WR)	12	DB5
6	E (RD)	13	DB6
7	DB0	14	DB7

NC: no connection

Location and dimensions (Diameter of holes is 1.0mm.) ※ The third through hole is for reset input when No 1 and No 2 of JP1 are short.

UNIT : mm

Notice for the Cautious Handling VFD Modules

Handling and Usage Precautions:

Please carefully follow the appropriate product application notes for proper usage, safety handling, and operation standards for maximum performance.

[VFD tubes are made of glass]

- Because the edges of the VFD glass-envelop are not smooth, it is necessary to handle carefully to avoid injuries to your hands
- Please avoid breaking the VFD glass-envelop to prevent injury from sharp glass particles.
- The tip of the exhaust pipe is fragile so avoid shock from impact.
- It is recommended to allow sufficient open space surrounding the exhaust pipe to avoid possible damage.
- Please design the PCB for the VFD-module within 0.3 mm warping tolerance to avoid any forces that may damage the display due to PCB distortion causing a breakdown of the electrical circuit leading to VFD failure.

[High voltage]

- Avoid touching conductive electrical parts, because the VFD-module uses high voltage exceeding 30 ~ 100 volts.
- Even when electric power is turned off, it may take more than one minute for the electrical current to discharge.
- [Cable connection]
 - Do not unplug the power and/or data cables of VFD-modules during operating condition because unrecoverable damage may result.
 - Sending input signals to the VFD-module during a power off condition sometimes causes I/O port damage.
 - It is recommended to use a 30 cm or shorter signal cable to prevent functional failures.

[Electrostatic charge]

- VFD-modules needs electrostatic free packaging and protection from electrostatic charges during handling and usage. [Structure]
 - During operation, VFD and VFD-modules generate heat. Please consider sufficient heat radiation dissipation using heat sink solutions.
 - We prefer to use UL grade materials or components in conjunction with VFD-modules.
 - Wrap and twist motion causes stress and may break VFDs & VFD modules. Please adhere to allowances within 0.3mm at the point of attachment.

[Power]

- Apply regulated power to the VFD-module within specified voltages to protect from failures.
- Because some VFD-modules may consume in rush current equal to twice the typical current at power-on timing, we recommend using a sufficient power capability and quick starting of the power regulator.
- VFD-module needs a specified voltage at the point of connection. Please use an adequate power cable to avoid a decrease in voltage. We also recommend inserting a power fuse for extra protection.

[Operating consideration]

- Illuminating phosphor will decrease in brightness during extended operation. If a fixed pattern illuminates for an extended period,(several hours), the phosphor efficiency will decrease compared to the non operating phosphor causing a non uniform brightness among pixels. Please consider programming the display patterns to use all phosphor segments evenly. Scrolling may be a consideration for a period of time to refresh the phosphor condition and improve even illumination to the pixels.
- We recommend using a signal cable 30cm or less to avoid some possible disturbances to the signal.

[Storage and operating environment]

- Please use VFD-modules under the recommended specified environmental conditions. Salty, sulfur and dusty environments may damage the VFD-module even during storage.
- [Discard]
 - Some VFDs contain a small amount of cadmium in the phosphor and lead in the solder. When discarding VFDs or VFD-modules, please adhere to governmental related laws or regulations.

[Others]

- Although the VFD-module is designed to be protected from electrical noise, please plan your circuitry to exclude as much noise as possible.
- Do not reconstruct or repair the VFD-module without our authorization. We cannot assure the quality or reliability of unauthorized reconstructed VFD-modules.

Notice:

- · We do not authorize the use of any patents that may be inherent in these specifications.
- Neither whole nor partial copying of these specifications are permitted without our approval.
- If necessary, please ask for assistance from our sales consultant.
- This product is not designed for military, aerospace, medical or other life-critical applications. If you choose to use this product for these applications, please ask us for prior consultation or we cannot take responsibility for problems that may occur.