S1D13513 LCD/TV Mobile Graphics Engine

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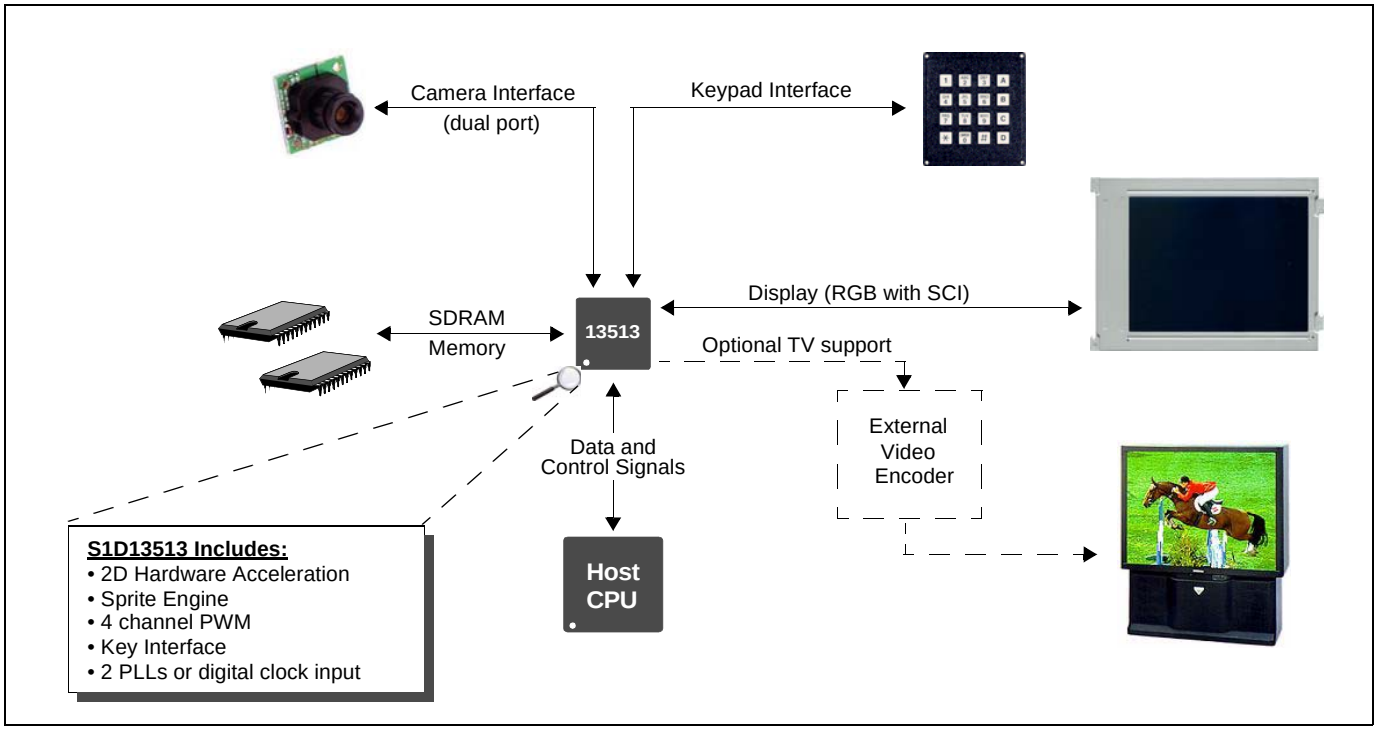
The S1D13513 is a highly integrated Mobile Graphics Engine capable of outputting to LCD or TV. With the flexibility of an external SDRAM memory interface, this low cost, low power, device supports a wide range of CPUs, panels, and provides a camera port that can be configured as 2x 8-bit ports, 1x 16-bit port, or alternately as a YUV output port. The S1D13513 feature set and architecture are designed to meet the requirements of embedded systems such as Mobile Communications, Hand-Held PC's, Office Automation, and Automotive applications.

The S1D13513 features both Sprite and 2D BitBLT engines designed to reduce the load on the Host, while increasing the performance of graphics intensive operations. Additionally, such features as SwivelView™, "Picture-In-Picture Plus", and EPSON Display technology allow user configurability of various images on the Main/PIP1/PIP2 displays. While focusing on devices targeted by the Microsoft Windows CE Operating System, the S1D13513's impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

FEATURES

- Direct and Indirect CPU interfaces
- Serial Host Interface
- Memory interface for x16 or x32 external SDRAM (x32 available on S1D13513 PBGA only)
- Programmable resolutions and color depths
- Support for single RGB panel with serial command interface
- TV support for YUV 4:2:2 output via external video encoder
- Clocks can be selected from two embedded PLLs or digital clock input
- Two built-in Crystal inputs
- Dual port Camera interface with resize function
- Overlay features
- 2D Hardware Acceleration Engine
- Sprite Engine
- SwivelView™ (90°, 180°, 270° hardware rotation of displayed image)
  - (Patent # 5,734,875 - Patent # 5,956,049 - Patent #6,262,751)
- "Picture-in-Picture Plus"
- 4 Channel PWM
- Software initiated Power Save Mode
- YUV to RGB converter
- Low Operating Voltage

SYSTEM BLOCK DIAGRAM



■ DESCRIPTION

External Display Buffer

- Uses external SDRAM or mobile SDRAM as display buffer
- Supports x16 SDRAM interface (Size: 8M byte, 16M byte, 32Mbyte or 64Mbyte)
- Supports x32 SDRAM interface (S1D13513 PBGA package only)
- Mobile SDRAM support
- SDRAM clock: 100 - 110MHz (TBD)
- Provides linear access to first 1M bytes and four configurable 256KB windows into the remaining memory

Display Support

- RGB Interface for single panel
- Color TFT Panel
- Color Passive Panel
- Serial Command interface
- TV (YUV Digital Output) support for YUV 4:2:2 output (NTSC or PAL format) via external Video Encoder
- Color Depths up to 32 bpp
- Example resolutions (TBD):
  1024x768 at a color depth of 16 bpp
  800x600 at a color depth of 16 bpp
  800x600 at a color depth of 16 bpp with PIP support

Display Features

- Layer/Window support using “Picture-in-Picture Plus”
- Horizontal Flip and Rotation (90/180/270°) using SwivelView[1]
  ([1] Refer to specification for SwivelView 90/270° restrictions)
- Double Buffering support
- Alpha Blending
- Gamma Correction
- Pseudo Color Expansion
- Hardware cursor support via the Sprite engine
- Camera image can be displayed on the PIP1/PIP2 window
- Interrupts available
  - Supports maskable non-display (Vsync) interrupt
  - Supports delayed version of Vsync Interrupt

CPU Interface

- Direct and indirect interface support for most popular CPU interfaces
- Serial Host Interface
- Registers are memory-mapped - M/R# input selects between memory and register address space

Digital Video

- Video Input port
  - Support for two 8-bit camera ports
  - 2nd camera port can be configured as a YUV output port
  - Supports CCIR-656 YUV format
  - Supports resize function of the video in stream
  - Supports raw JPEG capture from JPEG capable camera
- Captures YUV data into SDRAM as YUV 4:2:2 format
- View Image can be displayed to LCD or TV
- Resize function built-in for both View and Capture path

Acceleration

- 2D BitBLT Engine (Read, Write, Move, and Fill BLTs)
- 2D Sprite Engine (up to 16 sprites)
- Unified Command FIFO for both BitBLT and Sprite

Miscellaneous

- Host bus clock: TBD
- Internal system clock: TBD
- 4 channel PWM for backlight control
- I2C Interface
- Keypad Interface 5 x 5 matrix support
- Software initiated power save mode
- Clocks are dynamically turned off when modules are not needed
- Multiple General Purpose IO pins
- Clocks can be selected from two internal PLLs or digital clock input
- Two built-in crystal inputs
- $CORE_{VDD}$ 1.8 volts and IO_{VDD} 3.3 volts
- 208-pin QFP package and 256-pin PBGA package

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13513 Technical Documentation
- CPU Independent Software Utilities
- S1D13513 Evaluation Boards
- Royalty Free source level driver code

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