POWER MANAGEMENT SYSTEM DEVICE

RN5T567x-E4

Product Brief

Rev2.2

2022.1.1

This specification is subject to change without notice.

Nisshinbo Micro Devices Inc.

Table of Contents

1. Outline

This IC is the power management IC for GPS-PND/STB/POS/Panel Computer and so on.
It integrates four high-efficiency step-down DCDC converters, seven low dropout regulators, power control logic, I2C-Bus Interface, voltage detections, thermal shut-down, and etc.

2. Feature

●System
- ✓ I2C-Bus interface @3.4MHz and 400kHz
- ✓ Detector Function (System/IO, UVLO, DETVSB)
- ✓ Thermal Shutdown Function
- ✓ Watchdog timer
- ✓ Power on key input for System's power up
- ✓ Power on reset output for CPU
- ✓ Flexible power-on/off sequence by OTP
- ✓ Flexible DCDCx and LDOx default-on/off control by OTP

●High Efficiency Step-down DC/DC Converters
- ✓ DC/DC1 0.6-3.5V Max 3000mA
- ✓ DC/DC2 0.6-3.5V Max 3000mA
- ✓ DC/DC3 0.6-3.5V Max 2000mA
- ✓ DC/DC4 0.6-3.5V Max 2000mA
- ✓ Soft-start circuit

●Low Drop Voltage Regulators
- ✓ LDO1 0.9-3.5V Max 300mA
- ✓ LDO2 0.9-3.5V Max 300mA
- ✓ LDO3 0.6-3.5V Max 300mA
- ✓ LDO4 0.9-3.5V Max 200mA
- ✓ LDO5 0.9-3.5V Max 200mA
- ✓ LDORTC1 1.2-3.5V Max 30mA (AlwaysOn, For coin battery)
- ✓ LDORTC2 0.9-3.5V Max 10mA (AlwaysOn)
- ✓ Over current Protection and Short circuit Protection.

●4ch-GPIO
- ✓ Supports interrupt function (level/edge) for input signals
- ✓ Outputs power-on signal for external devices
- ✓ Power on/off input for System's power up/down
- ✓ DCDCx and LDOx can be controlled by external input
- ✓ GPIO2 can output LDORTC2
- ✓ GPIO0 and GPIO1 have maximum 15mA sink for LED.
- ✓ GPIOx have Output C32KOUT of internal clock for external devices.

●Interrupt Controller (INTC)
●Package QFN0606-48(0.4mm pitch)
●Process CMOS

3. Block Diagram

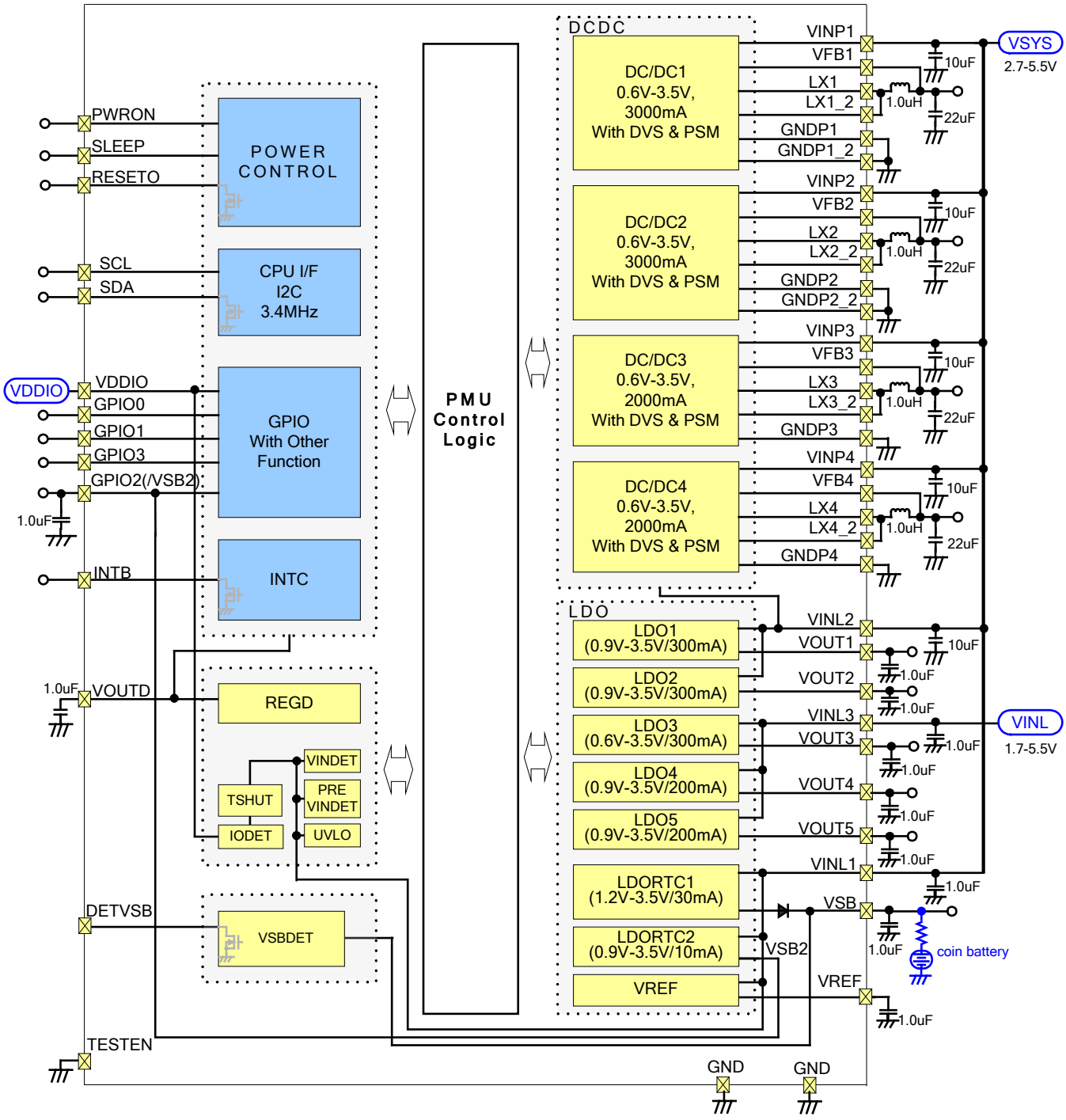

Fig 3-1 Block Diagram

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Exposure to the condition exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

Symbol	Parameter	Condition	Min	Max	Units
V_{PS1}	Power Supply Voltage 1	VINP1-4, VINL1-3pin	-0.3	6.0	V
V_{PS2}	Power Supply Voltage 2	VDDIO pin	-0.3	4.5	V
V_{INPUT}	Input Voltage Range	PWRON, SLEEP pin	-0.3	VINL1 + 0.3	V
		SDA, SCL pin	-0.3	4.5	V
		GPIO0-1 pin	-0.3	VINL1 + 0.3 / VDDIO + 0.3	V
		GPIO2-3 pin	-0.3	VINL1 + 0.3	V
V_{OUTPUT}	Output Voltage Range	RESETO, INTB,GPIO2-3 pin	-0.3	VINL1 + 0.3	V
		GPIO0-1 pin	-0.3	VINL1 + 0.3 / VDDIO + 0.3	V
		DETVSB pin	-0.3	VSB*+ 0.3	V
T_{stg}	Storage Temperature	-	-55	125	degrees C
PD	Package Allowable Dissipation	QFN0606-48(0.4mm pitch) T_a = 25 degrees C	0	3200	mW

*VSB : LDORTC1_Output or Coin Battery

Table 4-1 Absolute Maximum Ratings

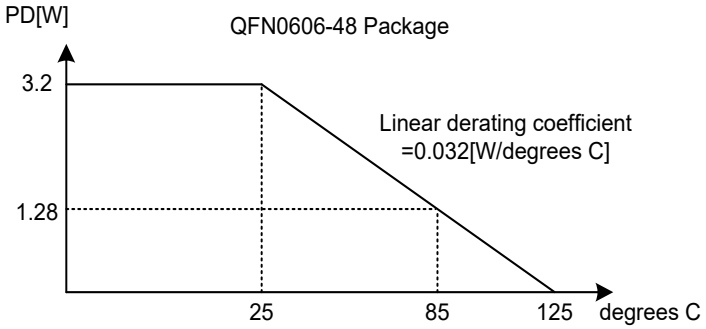

Fig 4-1 Maximum Package Allowable Dissipation

4.2 Recommendation of Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VSYS	Power Supply Voltage	VINP1-4, VINL1-2 pin *1	2.7	3.6	5.5	V
VINL	Power Supply Voltage	VINL3 pin *2	1.7	3.6	5.5	V
VDDIO	Power Supply Voltage	VDDIO pin (VSYS > VDDIO)	1.7	1.8	3.4	V
VSB	Power Supply Voltage	VSB pin	1.45	3.1	3.4	V
GND	Ground	GND		0		V
Ta	Temperature of Operation	-	-40		85	degrees C

Note*1:VINP1-4 and VINL2 must be equal to VINL1.
However, if POWROFF state, VINP1-4 and VINL2 is possible to power-off
(Only Parts Mode and then Input pin level must be GND.)
Note*2:VINL3 must be less than or equal to VINL1.

Table 4-2 Recommendation of Operating Conditions

4.3 I/O Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
VINL1 NMOS Input Pin: PWRON,SLEEP, GPIO0, GPIO1, GPIO2, GPIO3						
VIL	Low level input voltage				0.4	V
VIH	High level input voltage		1.4		VINL1	V
VINL1 Nch Open Drain output Pin : RESETO						
VOL	Low level output voltage	Iout = 2mA			0.4	V
Vto	Tolerant				VINL1	V
VINL1 CMOS input/output Pin : GPIO0, GPIO1, GPIO2, GPIO3						
VIL	Low level input voltage				VINL1*0.2	V
VIH	High level input voltage		VINL1*0.8		VINL1	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VINL1-0.4			V
VINL1 Nch Open Drain output Pin : INTB, GPIO0, GPIO1, GPIO2, GPIO3						
VOL	Low level output voltage	Iout = 4mA			0.4	V
Vto	Tolerant				VINL1	V
VINL1 Nch Open Drain output Pin: GPIO0, GPIO1 (for LED)						
VOL	Low level output voltage	Iout = 15mA			0.4	V
Vto	Tolerant				VINL1	V
VSB Nch Open Drain output Pin: DETVSB						
VOL	Low level output voltage	Iout = 1mA			0.2	V
Vto	Tolerant				VSB	V

Symbol	Parameter	Condition	Min	Typ	Max	Units
VOUTD CMOS input Pin (Schmitt Input): SCL						
VIL	Low level input voltage				VOUTD *0.3	V
VIH	High level input voltage		VOUTD *0.7		3.4	V
ΔVI	Hysteresis		VOUTD *0.1			V
VOUTD CMOS input/output Pin(Schmitt Input / Nch Open Drain output) : SDA						
VIL	Low level input voltage				VOUTD *0.3	V
VIH	High level input voltage		VOUTD *0.7		3.4	V
ΔVI	Hysteresis		VOUTD *0.1			V
VOL	Low level output voltage	Iout = 3mA			0.4	V
VDDIO CMOS input/output Pin : GPIO0, GPIO1						
VIL	Low level input voltage				VDDIO*0.2	V
VIH	High level input voltage		VDDIO*0.8		VDDIO	V
VOL	Low level output voltage	Iout = 4mA			0.4	V
VOH	High level output voltage	Iout = -4mA	VDDIO-0.4			V

*VOUTD : REGD_Output (1.8V)

Table 4-3 I/O Electrical Characteristics

4.4 Consumption Current

Operating Conditions (unless otherwise specified) T_a = 25 degrees C, V_{IN} =3.6V, No-load

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{ST}	Standby current	PowerOff (Note*1)		15		μA
I_{OP}	Operating current	PowerOn (Note*1)		350		μA
I_{SLP}	Sleep current	Sleep (Note*1)		100		μA

Table 4-4 Consumption Current

Note*1) Each condition is below. (It is possible to change the enabled LDO/DCDC at PowerOn/Sleep.)

	PowerOFF	PowerON	Sleep
LDO1	-	○	-
LDO2	-	○	-
LDO3	-	○	○
LDO4	-	○	○
LDO5	-	○	-
LDORTC1	○	○	○
LDORTC2	-	-	-
VREF	○	○	○
DCDC1	-	○	-
DCDC2	-	○	○(ECO)
DCDC3	-	-	-
DCDC4	-	-	-
UVLO	○	○	○
VINDET	○	○	○
IODET	○	○	○
PREVINDET	○	○	○
VSBDET	○	○	○
TSHUT	○	○	○
REGD	○	○	○
Internal Logic	○	○	○

5. Package information

5.1 Pin Configuration

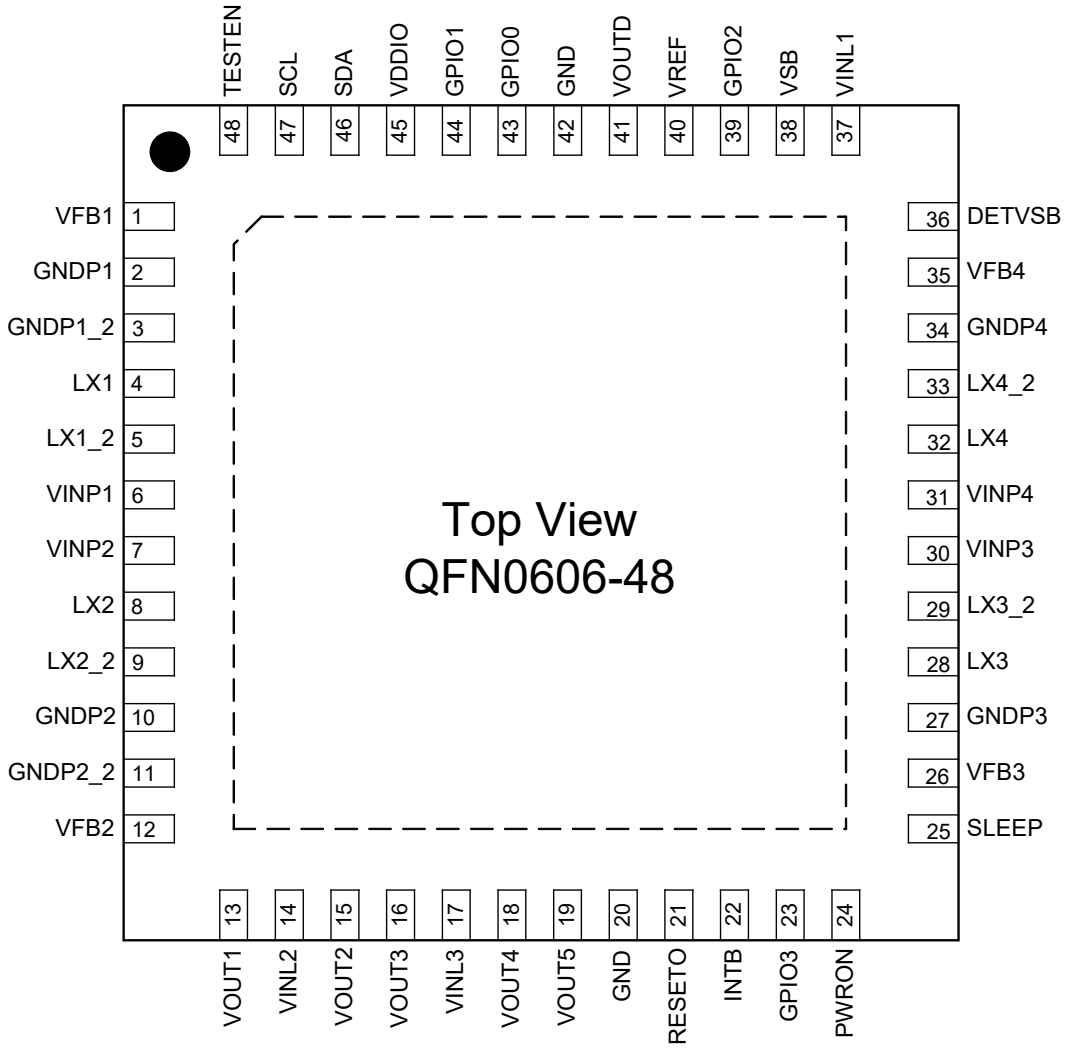

Fig 5-1 Pin Configuration

6. Pin Description

No.	Pin Name	Function	I/O (*1)	D/A (*2)	Reset State (*3)		Note
1	VFB1	DC/DC1 Output voltage feedback input	I/O	A			
2	GNDP1	GND for DC/DC1	-	G			
3	GNDP1_2	GND for DC/DC1	-	G			
4	LX1	DC/DC1 switch output	O	A			
5	LX1_2	DC/DC1 switch output	O	A			
6	VINP1	Power supply for DC/DC	-	P			
7	VINP2	Power supply for DC/DC2	-	P			
8	LX2	DC/DC2 switch output	O	A			
9	LX2_2	DC/DC2 switch output	O	A			
10	GNDP2	GND for DC/DC2	-	G			
11	GNDP2_2	GND for DC/DC2	-	G			
12	VFB2	DC/DC2 Output voltage feedback input	I/O	A			
13	VOUT1	LDO1 output	O	A			
14	VINL2	Power supply for LDO1,2 and DCDC analog	-	P			
15	VOUT2	LDO2 output	O	A			
16	VOUT3	LDO3 output	O	A			
17	VINL3	Power supply for LDO3,4 and LDO5	-	P			
18	VOUT4	LDO4 output	O	A			
19	VOUT5	LDO5 output	O	A			
20	GND	GND for Logic circuit,analog circuit, IO and etc	-	G			
21	RESETO	Host Reset output	O	D	O	Low	NOD
22	INTB	Interrupt request output	O	D	O	Hi-z	NOD
23	GPIO3	General purpose I/O Note*	I/O	D	*4	*4	*4
24	PWRON	External power on signal input	I	D	I	-	1.4V to VINL1
25	SLEEP	Stand-by mode control signal input	I	D	I	-	1.4V to VINL1
26	VFB3	DC/DC3 Output voltage feedback input	I/O	A			
27	GNDP3	GND for DC/DC3	-	G			
28	LX3	DC/DC3 switch output	O	A			
29	LX3_2	DC/DC3 switch output	O	A			
30	VINP3	Power supply for DC/DC3	-	P			
31	VINP4	Power supply for DC/DC4	-	P			
32	LX4	DC/DC4 switch output	O	A			
33	LX4_2	DC/DC4 switch output	O	A			
34	GNDP4	GND for DC/DC4	-	G			
35	VFB4	DC/DC4 Output voltage feedback input	I/O	A			
36	DETVSB	Voltage detection VSB output (Nch-opendrain)	O	D	O	-	NOD
37	VINL1	Power supply for LDORTC1,2, VREF, DET, IO and etc	-	P			
38	VSB	LDORTC1 output	O	A			
39	GPIO2(/VSB2)	General purpose I/O Note*	I/O	D	*4	*4	*4
40	VREF	Bypass capacitor connecting pin	O	A			
41	VOUTD	Capacitor connection for built-in Regulator	O	A			
42	GND	GND for Logic circuit,analog circuit, IO and etc	-	G			
43	GPIO0	General purpose I/O Note*	I/O	D	*4	*4	*4
44	GPIO1	General purpose I/O Note*	I/O	D	*4	*4	*4
45	VDDIO	Power supply for CPU IF	-	P			
46	SDA	I2C-Bus Data input/Output	I/O	D	I	-	Schmitt,NOD
47	SCL	I2C-Bus Clock input	I	D	I	-	CMOS
48	TESTEN	For TEST (Connect to GND)	I	D	I	PD	CMOS Schmitt

Note*1: I:Input, O:Output

Note*2: A:Analog, D:Digital, P:Power, G:Ground

Note*3: Reset State: RESETO=Low.

Note*4: GP00-GP03: "Input" or "Output" is selectable by OTP. Input/Output type (CMOS or NMOS or Analog or Nch Open Drain Output) is selectable by OTP. Refer to the chapter of GPIO for detail.

Table 6-1 Pin Description

7. Power Control

This PMU has the power-on/off sequence that can be flexibly set by OTP. The default on/off, timing, and voltage of DCDCx and LDOx are programmable. In addition, GPIO0-GPIO3 pins output the power-on/off signal to external LDO/DCDC by the setting of OTP.

7.1 State Machine Diagram

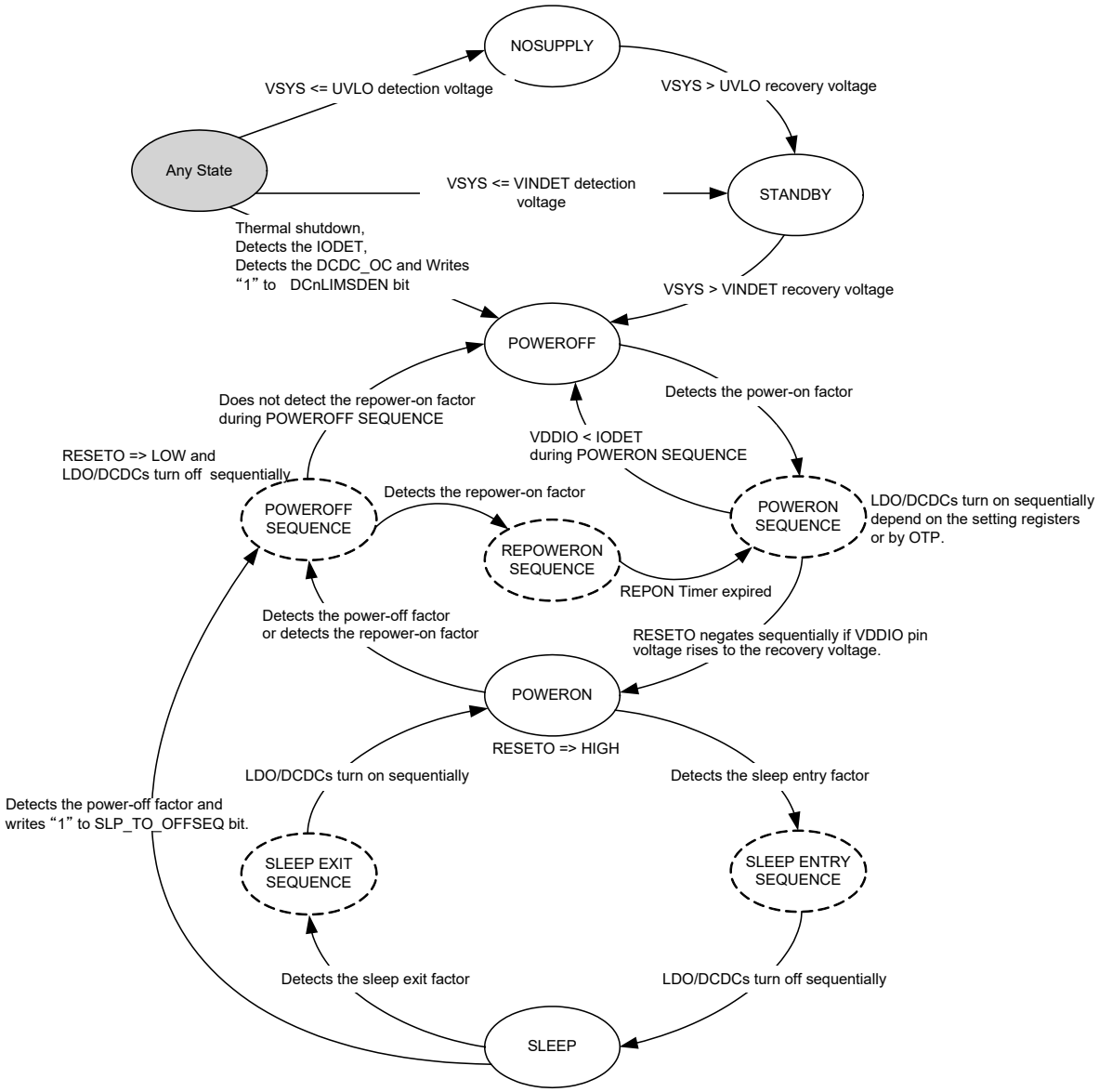

Fig 7-1 Power Control State Machine Diagram

8. Regulators

8.1 Regulators Table

Symbol	DCDC1	DCDC2	DCDC3	DCDC4
Initial Output Voltage	0.6-3.5V	0.6-3.5V	0.6-3.5V	0.6-3.5V
Maximum Output Current	3000mA	3000mA	2000mA	2000mA
External Inductor	1.0μH	1.0μH	1.0μH	1.0μH
External Capacitor	22μF	22μF	22μF	22μF
Output Control	I2C	I2C	I2C	I2C

Table 7-1 Regulator Table (DC/DC)

Symbol	LDO1	LDO2	LDO3	LDO4
Initial Output Voltage	0.9-3.5V	0.9-3.5V	0.6-3.5V	0.9-3.5V
Maximum Output Current	300mA	300mA	300mA	200mA
External Capacitor	1μF	1μF	1μF	1μF
Output Control	I2C	I2C	I2C	I2C

Symbol	LDO5	LDORTC1	LDORTC2	
Initial Output Voltage	0.9-3.5V	1.2-3.5V	0.9-3.5V	
Maximum Output Current	200mA	30mA	10mA	
External Capacitor	1μF	1uF	1uF	
Output Control	I2C	Always-On/I2C	Always-On/I2C	

Table 7-2 Regulator Table (LDO)

9. MODE

This PMU has two Modes selected by OTP.

MODE	Pin					
	GPIO0	GPIO1	GPIO2	GPIO3	SLEEP	PWRON
Normal	selectable				SLEEP	PWRON
Parts	DCDC1 EXON	DCDC2 EXON	DCDC3 EXON	DCDC4EXON and LDO3EXON	LDO1EXON and LDO4EXON	LDO2EXON and LDO5EXON

Table 9-1 Modes and function of pins

9.1 Normal MODE

The function of GPIO0-3 pins can be respectively selected by OTP. Note*
The function of SLEEP and PWRON pins are respectively decided SLEEP and PWRON.

Note*: For details of the function of GPIO* pins, refer to GPIO.

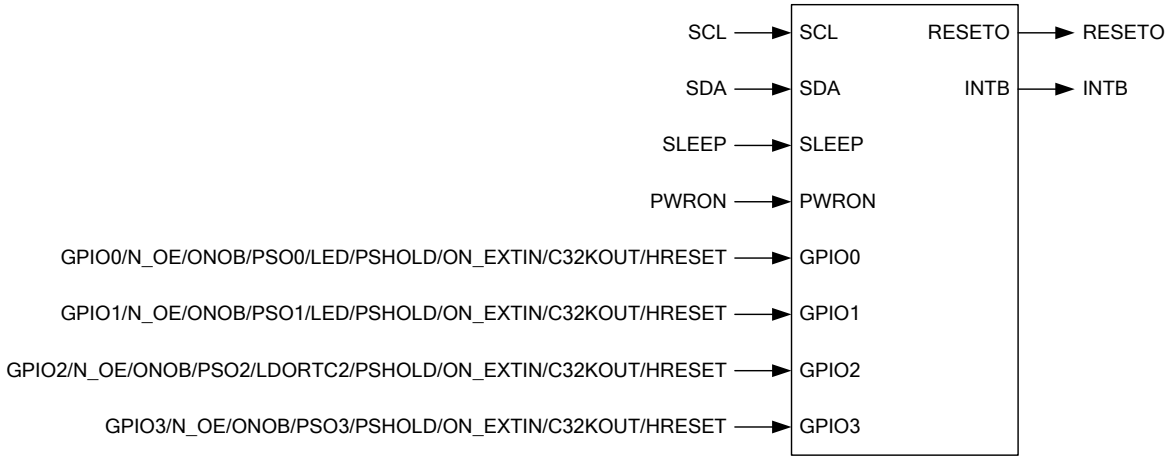

Fig 9-1 The function of pins in Normal mode

9.2 Parts MODE

ON/OFF of DCDC1-4 and LDO1-5 can be controlled by pin.

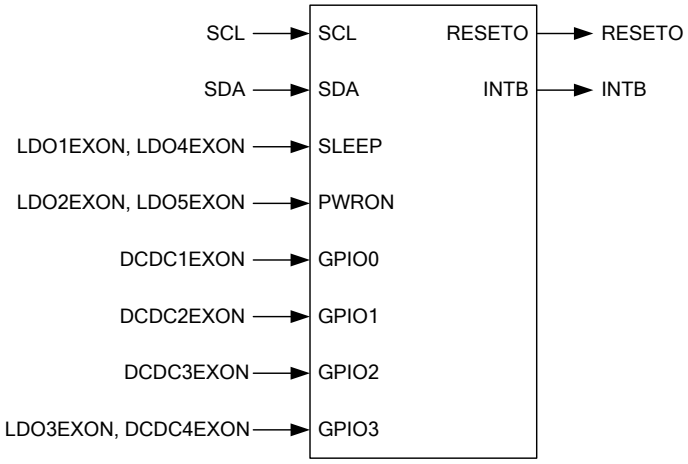

Fig 9-2 The function of pins in Parts mode

10. GPIO

This PMU supports four channels of general purpose input/output.
GPIO0-3 pins have the function selected by OTP as shown below.

Name	Function	Input,*1,*2	Output,*1,*2	Power,*3	GPIO			
					0	1	2	3
N_OE	External power off	N	-	VSYS	○	○	○	○
GPIO0	General purpose I/O	C or N	C or N	VSYS or VDDIO	○	-	-	-
GPIO1	General purpose I/O	C or N	C or N	VSYS or VDDIO	-	○	-	-
GPIO2	General purpose I/O	C or N	C or N	VSYS	-	-	○	-
GPIO3	General purpose I/O	C or N	C or N	VSYS	-	-	-	○
ONOB	PWRON pin monitor	-	N	VSYS	○	○	○	○
PSO0	Power-on signal output function	-	C or N	VSYS or VDDIO	○	-	-	-
PSO1	Power-on signal output function	-	C or N	VSYS or VDDIO	-	○	-	-
PSO2	Power-on signal output function	-	C or N	VSYS	-	-	○	-
PSO3	Power-on signal output function	-	C or N	VSYS	-	-	-	○
LDORTC2	LDORTC2 output	-	A	-	-	-	○	-
LED	LED function	-	N	VSYS	○	○	-	-
PSHOLD	PSHOLD (power-on hold) function	N	-	VSYS	○	○	○	○
ON_EXTIN	External input for on factor	N	-	VSYS	○	○	○	○
**EXON	External LDO*/DCDC* on/off input	N	-	VSYS	*4	*4	*4	*4
C32KOUT	32 kHz clock output function	-	C or N	VSYS or VDDIO	○	○	○	○
HRESET	Hard RESET input	N	-	VSYS	○	○	○	○

Note*1: Explanation of column of “Input” and “Output” :
A : Analog Output.
C : CMOS Input/Output.
N : NMOS Input(VSYS only)/ Nch Open Drain Output.
Note*2: CMOS or Nch is selectable by OTP.
Note*3: VSYS or VDDIO is selectable by OTP.
Note*4: Refer to the chapter of Mode.

Table 10-1 The function of GPIO0-3 pins

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